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FSTUD32450 Configurable 4-Bit to 40-Bit Bus Switch with -2V Undershoot Protection and Selectable Level Shifting

FSTUD32450

Configurable 4-Bit to 40-Bit Bus Switch with -2V Undershoot Protection and Selectable Level Shifting

General Description

The Fairchild Universal Bus Switch FSTUD32450 provides 4-bit, 5-bit, 8-bit, 10-bit, 16-bit, 20-bit...40-bit of high-speed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The FSTUD32450 is designed to allow "customer" configuration control of the enable connections. The device can be organized as either a ten 4-bit, eight 5-bit, four 10-bit, two 20-bit or one 40-bit enabled bus switch. Also achievable are 8-bit and 16-bit enabled configurations (see Functional Description). The device's bit configuration is controlled through select pin logic. (see Truth Table). When \overline{OE}_x is LOW, Port A_x is connected to Port B_x . When \overline{OE}_x is HIGH, the switch is OPEN.

The A and B Ports are protected against undershoot to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHC[®]) senses undershoot at the I/O, and responds by preventing voltage differentials from developing and turning the switch on.

Another innovative device feature is the addition of a level shifting select pin, "S₂ and S₅". When S₂ and S₅ are LOW, the device behaves as a standard N-MOS switch. When S₂ and S₅ are HIGH, a diode to V_{CC} is integrated into the circuit allowing for level shifting between 5V inputs and 3.3V outputs.

Features

- Undershoot protected to -2V (A and B Ports)
- Voltage level shifting
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- See Applications Notes AN-5008 and AN-5021 for UHC details
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Applications Note

Select pins S₀, S₁, S₂, S₃, S₄ and S₅ are intended to be used as static user configurable control pins. The AC performance of these pins has not been characterized or tested. Switching of these select pins during system operation may temporarily disrupt output logic states and/or enable pin controls.

40-bit configuration can be achieved by connecting the \overline{OE}_1 and the \overline{OE}_6 pins to together.

Ordering Code:

| Order Number | Package Number | Package Description |
|---------------------------------|----------------|--|
| FSTUD32450G (Note 1)(Note 2) | BGA114A | 114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide |

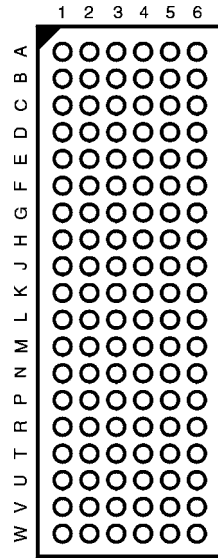
Note 1: Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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Connection Diagram

Pin Assignment for FBGA



(Top Thru View)

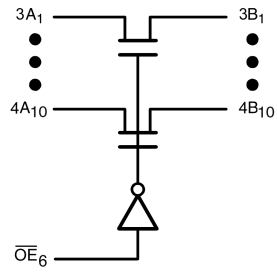
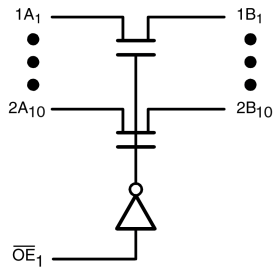
Pin Descriptions

| Pin Name | Description |
|---|------------------------------|
| $\overline{OE}_1, \overline{OE}_2, \overline{OE}_3, \overline{OE}_4,$ $\overline{OE}_5, \overline{OE}_6, \overline{OE}_7, \overline{OE}_8$ | Bus Switch |
| $\overline{OE}_9, \overline{OE}_{10}$ | Enables |
| 1A, 2A, 3A, 4A | Bus A |
| 1B, 2B, 3B, 4B | Bus B |
| S ₀ , S ₁ , S ₃ , S ₄ | Bit Configuration Enables |
| S ₂ , S ₅ | Level Shifting Diode Enables |

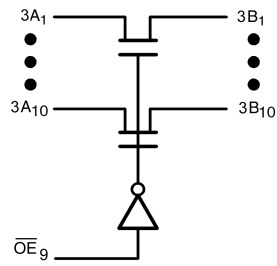
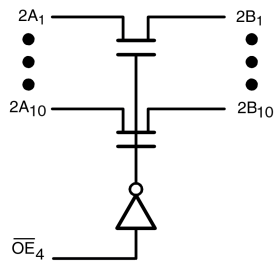
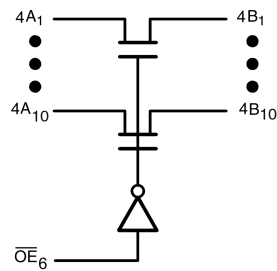
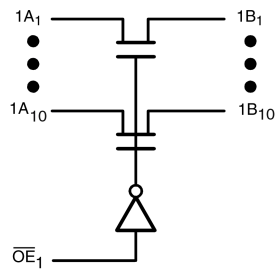
FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-------------------|-------------------|----------------------|-------------------|-------------------|-------------------|
| A | 1A ₄ | 1A ₂ | \overline{OE}_1 | \overline{OE}_2 | 1B ₂ | 1B ₄ |
| B | 1A ₆ | 1A ₅ | 1A ₁ | 1B ₁ | 1B ₅ | 1B ₆ |
| C | 1A ₈ | 1A ₇ | 1A ₃ | 1B ₃ | 1B ₇ | 1B ₈ |
| D | 1A ₁₀ | 1A ₉ | GND | \overline{OE}_5 | 1B ₉ | 1B ₁₀ |
| E | 2A ₂ | 2A ₁ | S ₀ | V _{CC} | 2B ₁ | 2B ₂ |
| F | 2A ₄ | 2A ₃ | S ₁ | S ₂ | 2B ₃ | 2B ₄ |
| G | 2A ₆ | 2A ₅ | V _{CC} | GND | 2B ₅ | 2B ₆ |
| H | 2A ₈ | 2A ₇ | GND | GND | 2B ₇ | 2B ₈ |
| J | 2A ₁₀ | 2A ₉ | GND | GND | 2B ₉ | 2B ₁₀ |
| K | \overline{OE}_4 | \overline{OE}_8 | GND | GND | \overline{OE}_9 | \overline{OE}_3 |
| L | 3A ₁₀ | 3A ₉ | GND | GND | 3B ₉ | 3B ₁₀ |
| M | 3A ₈ | 3A ₇ | GND | GND | 3B ₇ | 3B ₈ |
| N | 3A ₆ | 3A ₅ | GND | V _{CC} | 3B ₅ | 3B ₆ |
| P | 3A ₄ | 3A ₃ | S ₅ | S ₄ | 3B ₃ | 3B ₄ |
| R | 3A ₂ | 3A ₁ | V _{CC} | S ₃ | 3B ₁ | 3B ₂ |
| T | 4A ₁₀ | 4A ₉ | \overline{OE}_{10} | GND | 4B ₉ | 4B ₁₀ |
| U | 4A ₈ | 4A ₇ | 4A ₃ | 4B ₃ | 4B ₇ | 4B ₈ |
| V | 4A ₆ | 4A ₅ | 4A ₁ | 4B ₁ | 4B ₅ | 4B ₆ |
| W | 4A ₄ | 4A ₂ | \overline{OE}_7 | \overline{OE}_6 | 4B ₂ | 4B ₄ |

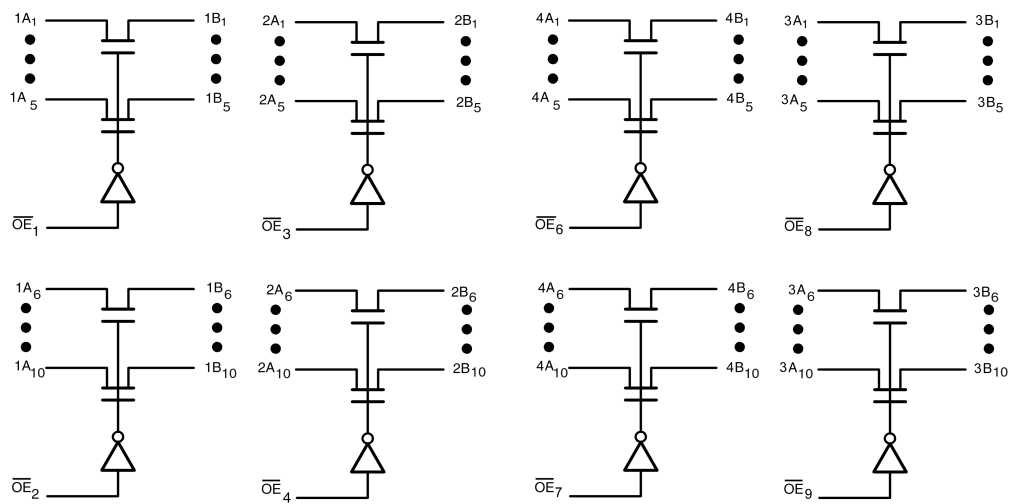
Logic Diagrams



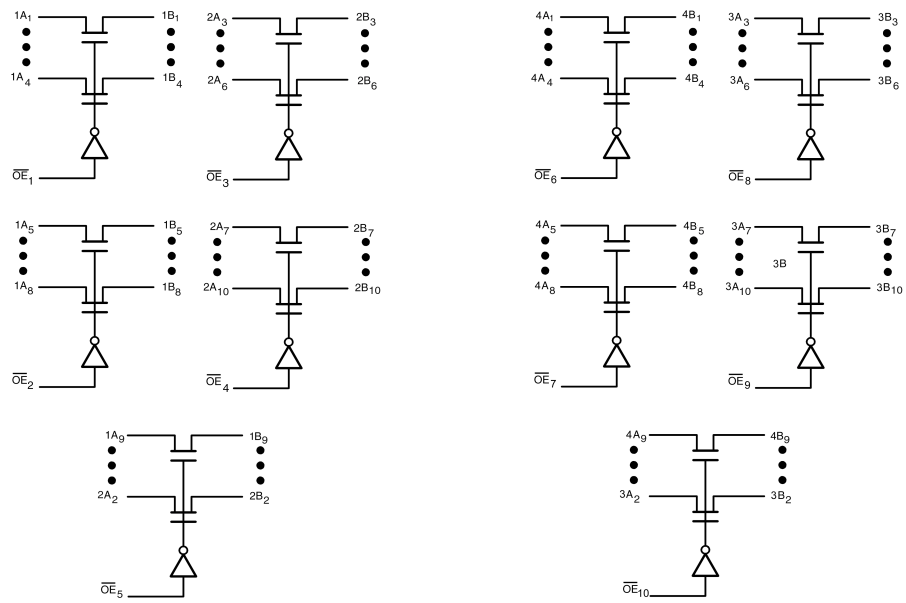
20-Bit Configuration



10-Bit Configuration



5-Bit Configuration



4-Bit Configuration

Functional Description

The device can also be configured as an 8 and 16-bit device by grounding the unused pins in Configurations 2 and 1 respectively. The 8-bit configuration may also be achieved by tying two of the 4-bit enables from configuration together and tying the remaining enable pin (\overline{OE}) HIGH.

Truth Tables (X = V_{CC} or GND)

(see Functional Description)

| Select Pin | |
|------------|------------------------------|
| S_2, S_5 | Mode |
| L | Std. NMOS Switch |
| H | Level Shifting Diode Enabled |

20-Bit Configuration ($S_0 = S_1 = L$)

| Inputs | | | | | Inputs/Outputs |
|-------------------|-------------------|-------------------|-------------------|----------------------|--|
| \overline{OE}_1 | \overline{OE}_2 | \overline{OE}_3 | \overline{OE}_4 | \overline{OE}_5 | |
| L | X | X | X | X | $1A_{1-10} = 1B_{1-10}, 2A_{1-10} = 2B_{1-10}$ |
| H | X | X | X | X | Z |
| $S_3 = S_4 = L$ | | | | | |
| Inputs | | | | | Inputs/Outputs |
| \overline{OE}_6 | \overline{OE}_7 | \overline{OE}_8 | \overline{OE}_9 | \overline{OE}_{10} | |
| L | X | X | X | X | $3A_{1-10} = 3B_{1-10}, 4A_{1-10} = 4B_{1-10}$ |
| H | X | X | X | X | Z |

10-Bit Configuration ($S_0 = L, S_1 = H$)

| Inputs | | | | | Inputs/Outputs | |
|--------------------|-------------------|-------------------|-------------------|----------------------|-------------------------|-------------------------|
| \overline{OE}_1 | \overline{OE}_2 | \overline{OE}_3 | \overline{OE}_4 | \overline{OE}_5 | $1A_{1-10} = 1B_{1-10}$ | $2A_{1-10} = 2B_{1-10}$ |
| L | X | X | L | X | $1A_X = 1B_X$ | $2A_X = 2B_X$ |
| L | X | X | H | X | $1A_X = 1B_X$ | Z |
| H | X | X | L | X | Z | $2A_X = 2B_X$ |
| H | X | X | H | X | Z | Z |
| $S_3 = L, S_4 = H$ | | | | | | |
| Inputs | | | | | Inputs/Outputs | |
| \overline{OE}_6 | \overline{OE}_7 | \overline{OE}_8 | \overline{OE}_9 | \overline{OE}_{10} | $4A_{1-10} = 4B_{1-10}$ | $3A_{1-10} = 3B_{1-10}$ |
| L | X | X | L | X | $4A_X = 4B_X$ | $3A_X = 3B_X$ |
| L | X | X | H | X | $4A_X = 4B_X$ | Z |
| H | X | X | L | X | Z | $3A_X = 3B_X$ |
| H | X | X | H | X | Z | Z |

Truth Tables (Continued)

5-Bit Configuration ($S_0 = H, S_1 = L$)

| Inputs | | | | | Inputs/Outputs | | | |
|---|-------------------|-------------------|-------------------|----------------------|---------------------------------------|---|---------------------------------------|---|
| \overline{OE}_1 | \overline{OE}_2 | \overline{OE}_3 | \overline{OE}_4 | \overline{OE}_5 | 1A ₁₋₅ , 1B ₁₋₅ | 1A ₆₋₁₀ , 1B ₆₋₁₀ | 2A ₁₋₅ , 2B ₁₋₅ | 2A ₆₋₁₀ , 2B ₆₋₁₀ |
| L | L | L | L | X | 1A _x = 1B _x | 1A _y = 1B _y | 2A _x = 2B _x | 2A _y = 2B _y |
| L | L | L | H | X | 1A _x = 1B _x | 1A _y = 1B _y | 2A _x = 2B _x | Z |
| L | L | H | L | X | 1A _x = 1B _x | 1A _y = 1B _y | Z | 2A _y = 2B _y |
| L | L | H | H | X | 1A _x = 1B _x | 1A _y = 1B _y | Z | Z |
| L | H | L | L | X | 1A _x = 1B _x | Z | 2A _x = 2B _x | 2A _y = 2B _y |
| L | H | L | H | X | 1A _x = 1B _x | Z | 2A _x = 2B _x | Z |
| L | H | H | L | X | 1A _x = 1B _x | Z | Z | 2A _y = 2B _y |
| L | H | H | H | X | 1A _x = 1B _x | Z | Z | Z |
| H | L | L | L | X | Z | 1A _y = 1B _y | 2A _x = 2B _x | 2A _y = 2B _y |
| H | L | L | H | X | Z | 1A _y = 1B _y | 2A _x = 2B _x | Z |
| H | L | H | L | X | Z | 1A _y = 1B _y | Z | 2A _y = 2B _y |
| H | L | H | H | X | Z | 1A _y = 1B _y | Z | Z |
| H | H | L | L | X | Z | Z | 2A _x = 2B _x | 2A _y = 2B _y |
| H | H | L | H | X | Z | Z | 2A _x = 2B _x | Z |
| H | H | H | L | X | Z | Z | Z | 2A _y = 2B _y |
| H | H | H | H | X | Z | Z | Z | Z |
| S₃ = H, S₄ = L | | | | | | | | |
| Inputs | | | | | Inputs/Outputs | | | |
| \overline{OE}_6 | \overline{OE}_7 | \overline{OE}_8 | \overline{OE}_9 | \overline{OE}_{10} | 4A ₁₋₅ , 4B ₁₋₅ | 4A ₆₋₁₀ , 4B ₆₋₁₀ | 3A ₁₋₅ , 3B ₁₋₅ | 3A ₆₋₁₀ , 3B ₆₋₁₀ |
| L | L | L | L | X | 4A _x = 4B _x | 4A _y = 4B _y | 3A _x = 3B _x | 3A _y = 3B _y |
| L | L | L | H | X | 4A _x = 4B _x | 4A _y = 4B _y | 3A _x = 3B _x | Z |
| L | L | H | L | X | 4A _x = 4B _x | 4A _y = 4B _y | Z | 3A _y = 3B _y |
| L | L | H | H | X | 4A _x = 4B _x | 4A _y = 4B _y | Z | Z |
| L | H | L | L | X | 4A _x = 4B _x | Z | 3A _x = 3B _x | 3A _y = 3B _y |
| L | H | L | H | X | 4A _x = 4B _x | Z | 3A _x = 3B _x | Z |
| L | H | H | L | X | 4A _x = 4B _x | Z | Z | 3A _y = 3B _y |
| L | H | H | H | X | 4A _x = 4B _x | Z | Z | Z |
| H | L | L | L | X | Z | 4A _y = 4B _y | 3A _x = 3B _x | 3A _y = 3B _y |
| H | L | L | H | X | Z | 4A _y = 4B _y | 3A _x = 3B _x | Z |
| H | L | H | L | X | Z | 4A _y = 4B _y | Z | 3A _y = 3B _y |
| H | L | H | H | X | Z | 4A _y = 4B _y | Z | Z |
| H | H | L | L | X | Z | Z | 3A _x = 3B _x | 3A _y = 3B _y |
| H | H | L | H | X | Z | Z | 3A _x = 3B _x | Z |
| H | H | H | L | X | Z | Z | Z | 3A _y = 3B _y |
| H | H | H | H | X | Z | Z | Z | Z |

Truth Tables (Continued)

4-Bit Configuration ($S_0 = S_1 = H$)

| Inputs | | | | | Inputs/Outputs | | | | |
|-----------------|-----------------|-----------------|-----------------|-----------------|---------------------------------------|---------------------------------------|---------------------------------------|---|--|
| OE ₁ | OE ₂ | OE ₃ | OE ₄ | OE ₅ | 1A ₁₋₄ , 1B ₁₋₄ | 1A ₅₋₈ , 1B ₅₋₈ | 2A ₃₋₆ , 2B ₃₋₆ | 2A ₇₋₁₀ , 2B ₇₋₁₀ | 1A ₉₋₁₀ , 2B ₉₋₁₀ 2A ₁₋₂ , 2B ₁₋₂ |
| L | L | L | L | L | 1A _x = 1B _x | 1A _y = 1B _y | 2A _x = 2B _x | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| L | L | L | L | H | 1A _x = 1B _x | 1A _y = 1B _y | 2A _x = 2B _x | 2A _y = 2B _y | Z |
| L | L | L | H | L | 1A _x = 1B _x | 1A _y = 1B _y | 2A _x = 2B _x | Z | 1A _z = 1B _z 2A _z = 2B _z |
| L | L | L | H | H | 1A _x = 1B _x | 1A _y = 1B _y | 2A _x = 2B _x | Z | Z |
| L | L | H | L | L | 1A _x = 1B _x | 1A _y = 1B _y | Z | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| L | L | H | L | H | 1A _x = 1B _x | 1A _y = 1B _y | Z | 2A _y = 2B _y | Z |
| L | L | H | H | L | 1A _x = 1B _x | 1A _y = 1B _y | Z | Z | 1A _z = 1B _z 2A _z = 2B _z |
| L | L | H | H | H | 1A _x = 1B _x | 1A _y = 1B _y | Z | Z | Z |
| L | H | L | L | L | 1A _x = 1B _x | Z | 2A _x = 2B _x | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| L | H | L | L | H | 1A _x = 1B _x | Z | 2A _x = 2B _x | 2A _y = 2B _y | Z |
| L | H | L | H | L | 1A _x = 1B _x | Z | 2A _x = 2B _x | Z | 1A _z = 1B _z 2A _z = 2B _z |
| L | H | L | H | H | 1A _x = 1B _x | Z | 2A _x = 2B _x | Z | Z |
| L | H | H | L | L | 1A _x = 1B _x | Z | Z | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| L | H | H | L | H | 1A _x = 1B _x | Z | Z | 2A _y = 2B _y | Z |
| L | H | H | H | L | 1A _x = 1B _x | Z | Z | Z | 1A _z = 1B _z 2A _z = 2B _z |
| L | H | H | H | H | 1A _x = 1B _x | Z | Z | Z | Z |
| H | L | L | L | L | Z | 1A _y = 1B _y | 2A _x = 2B _x | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| H | L | L | L | H | Z | 1A _y = 1B _y | 2A _x = 2B _x | 2A _y = 2B _y | Z |
| H | L | L | H | L | Z | 1A _y = 1B _y | 2A _x = 2B _x | Z | 1A _z = 1B _z 2A _z = 2B _z |
| H | L | L | H | H | Z | 1A _y = 1B _y | 2A _x = 2B _x | Z | Z |
| H | L | H | L | L | Z | 1A _y = 1B _y | Z | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| H | L | H | L | H | Z | 1A _y = 1B _y | Z | 2A _y = 2B _y | Z |
| H | L | H | H | L | Z | 1A _y = 1B _y | Z | Z | 1A _z = 1B _z 2A _z = 2B _z |
| H | L | H | H | H | Z | 1A _y = 1B _y | Z | Z | Z |
| H | H | L | L | L | Z | Z | 2A _x = 2B _x | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| H | H | L | L | H | Z | Z | 2A _x = 2B _x | 2A _y = 2B _y | Z |
| H | H | L | H | L | Z | Z | 2A _x = 2B _x | Z | 1A _z = 1B _z 2A _z = 2B _z |
| H | H | L | H | H | Z | Z | 2A _x = 2B _x | Z | Z |
| H | H | H | L | L | Z | Z | Z | 2A _y = 2B _y | 1A _z = 1B _z 2A _z = 2B _z |
| H | H | H | L | H | Z | Z | Z | 2A _y = 2B _y | Z |
| H | H | H | H | L | Z | Z | Z | Z | 1A _z = 1B _z 2A _z = 2B _z |
| H | H | H | H | H | Z | Z | Z | Z | Z |

Truth Tables (Continued)

4-Bit Configuration (continued)

| $S_3 = S_4 = H$ | | | | | | | | | |
|-----------------|--------|--------|--------|-----------|----------------------|----------------------|----------------------|------------------------|--|
| Inputs | | | | | Inputs/Outputs | | | | |
| OE_6 | OE_7 | OE_8 | OE_9 | OE_{10} | $4A_{1-4}, 4B_{1-4}$ | $4A_{5-8}, 4B_{5-8}$ | $3A_{3-6}, 3B_{3-6}$ | $3A_{7-10}, 3B_{7-10}$ | $3A_{1-2}, 3B_{1-2}$ $4A_{9-10}, 3B_{9-10}$ |
| L | L | L | L | L | $4A_x = 4B_x$ | $4A_y = 4B_y$ | $3A_x = 3B_x$ | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | L | L | L | H | $4A_x = 4B_x$ | $4A_y = 4B_y$ | $3A_x = 3B_x$ | $3A_y = 3B_y$ | Z |
| L | L | L | H | L | $4A_x = 4B_x$ | $4A_y = 4B_y$ | $3A_x = 3B_x$ | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | L | L | H | H | $4A_x = 4B_x$ | $4A_y = 4B_y$ | $3A_x = 3B_x$ | Z | Z |
| L | L | H | L | L | $4A_x = 4B_x$ | $4A_y = 4B_y$ | Z | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | L | H | L | H | $4A_x = 4B_x$ | $4A_y = 4B_y$ | Z | $3A_y = 3B_y$ | Z |
| L | L | H | H | L | $4A_x = 4B_x$ | $4A_y = 4B_y$ | Z | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | L | H | H | H | $4A_x = 4B_x$ | $4A_y = 4B_y$ | Z | Z | Z |
| L | H | L | L | L | $4A_x = 4B_x$ | Z | $3A_x = 3B_x$ | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | H | L | L | H | $4A_x = 4B_x$ | Z | $3A_x = 3B_x$ | $3A_y = 3B_y$ | Z |
| L | H | L | H | L | $4A_x = 4B_x$ | Z | $3A_x = 3B_x$ | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | H | L | H | H | $4A_x = 4B_x$ | Z | $3A_x = 3B_x$ | Z | Z |
| L | H | H | L | L | $4A_x = 4B_x$ | Z | Z | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | H | H | L | H | $4A_x = 4B_x$ | Z | Z | $3A_y = 3B_y$ | Z |
| L | H | H | H | L | $4A_x = 4B_x$ | Z | Z | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| L | H | H | H | H | $4A_x = 4B_x$ | Z | Z | Z | Z |
| H | L | L | L | L | Z | $4A_y = 4B_y$ | $3A_x = 3B_x$ | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | L | L | L | H | Z | $4A_y = 4B_y$ | $3A_x = 3B_x$ | $3A_y = 3B_y$ | Z |
| H | L | L | H | L | Z | $4A_y = 4B_y$ | $3A_x = 3B_x$ | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | L | L | H | H | Z | $4A_y = 4B_y$ | $3A_x = 3B_x$ | Z | Z |
| H | L | H | L | L | Z | $4A_y = 4B_y$ | Z | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | L | H | L | H | Z | $4A_y = 4B_y$ | Z | $3A_y = 3B_y$ | Z |
| H | L | H | H | L | Z | $4A_y = 4B_y$ | Z | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | L | H | H | H | Z | $4A_y = 4B_y$ | Z | Z | Z |
| H | H | L | L | L | Z | Z | $3A_x = 3B_x$ | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | H | L | L | H | Z | Z | $3A_x = 3B_x$ | $3A_y = 3B_y$ | Z |
| H | H | L | H | L | Z | Z | $3A_x = 3B_x$ | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | H | L | H | H | Z | Z | $3A_x = 3B_x$ | Z | Z |
| H | H | H | L | L | Z | Z | Z | $3A_y = 3B_y$ | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | H | H | L | H | Z | Z | Z | $3A_y = 3B_y$ | Z |
| H | H | H | H | L | Z | Z | Z | Z | $3A_z = 3B_z$ $4A_z = 4B_z$ |
| H | H | H | H | H | Z | Z | Z | Z | Z |

Absolute Maximum Ratings (Note 3)

| | |
|--|------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Switch Voltage (V_S) (Note 4) | -2.0V to +7.0V |
| DC Input Control Pin Voltage (V_{IN}) (Note 5) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) $V_{IN} < 0V$ | -50 mA |
| DC Output (I_{OUT}) Current | 128 mA |
| DC V_{CC}/GND Current (I_{CC}/I_{GND}) | +/- 100 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150 °C |

Recommended Operating Conditions (Note 6)

| | |
|--|------------------|
| Power Supply Operating (V_{CC}) | 4.0V to 5.5V |
| Input Voltage (V_{IN}) | 0V to 5.5V |
| Output Voltage (V_{OUT}) | 0V to 5.5V |
| Free Air Operating Temperature (T_A) | -40 °C to +85 °C |

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 5: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 6: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ | | | Units | Conditions |
|-----------|--|-----------------|---|-----------------|-----------|---------------|--|
| | | | Min | Typ (Note 7) | Max | | |
| V_{IK} | Clamp Diode Voltage | 4.5 | | | -1.2 | V | $I_{IN} = -18\text{ mA}$ |
| V_{IH} | HIGH Level Input Voltage | 4.0-5.5 | 2.0 | | | V | IF $S_2 = \text{HIGH}$ $4.5V \leq V_{CC} \leq 5.5V$ |
| V_{IL} | LOW Level Input Voltage | 4.0-5.5 | | | 0.8 | V | IF $S_2 = \text{HIGH}$ $4.5V \leq V_{CC} \leq 5.5V$ |
| V_{OH} | HIGH Level Output Voltage | 4.5-5.5 | See Figure 4 | | | V | $S_2 = S_5 = V_{CC}$ |
| I_I | Input Leakage Current | 5.5 | | | ± 1.0 | μA | $0 \leq V_{IN} \leq 5.5V$ |
| | | 0 | | | 10 | μA | $V_{IN} = 5.5V$ |
| I_{OZ} | OFF-STATE Leakage Current | 5.5 | | | ± 1.0 | μA | $0 \leq A, B \leq V_{CC}$ |
| R_{ON} | Switch On Resistance (Note 8) | 4.5 | | 4 | 7 | Ω | $V_{IN} = 0V, I_{IN} = 64\text{ mA}, S_2 = S_5 = 0V\text{ or }V_{CC}$ |
| | | 4.5 | | 4 | 7 | Ω | $V_{IN} = 0V, I_{IN} = 30\text{ mA}, S_2 = S_5 = 0V\text{ or }V_{CC}$ |
| | | 4.5 | | 8 | 12 | Ω | $V_{IN} = 2.4V, I_{IN} = 15\text{ mA}, S_2 = S_5 = 0V$ |
| | | 4.0 | | 11 | 20 | Ω | $V_{IN} = 2.4V, I_{IN} = 15\text{ mA}, S_2 = S_5 = 0V$ |
| | | 4.5 | | 35 | 50 | Ω | $V_{IN} = 2.4V, I_{IN} = 15\text{ mA}, S_2 = S_5 = V_{CC}$ |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 3 | μA | $S_2 = S_5 = \text{GND}, V_{IN} = V_{CC}\text{ or GND}, I_{OUT} = 0$ |
| | | | | | 10 | μA | $S_2 = S_5 = V_{CC}, \overline{OE}_x = V_{CC}, V_{IN} = V_{CC}\text{ or GND}, I_{OUT} = 0$ |
| | | | | | 1.5 | mA | $S_2 = S_5 = V_{CC}, \overline{OE}_x = \text{GND}, V_{IN} = V_{CC}\text{ or GND}, I_{OUT} = 0$ |
| I_{CCT} | Increase in I_{CC} per Control Input | 5.5 | | | 2.5 | mA | One Control Input at 3.4V Other Inputs at V_{CC} or GND, $S_2 = 0V$ |
| | | | | | 4.0 | mA | One Control Input at 3.4V Other Inputs at V_{CC} or GND, $S_2 = V_{CC}$ |
| V_{IKU} | Voltage Undershoot | 5.5 | | | -2.0 | V | $0.0\text{ mA} \geq I_{IN} \geq -50\text{ mA}$ $\overline{OE}_x = 5.5V$ |

Note 7: Typical values are at $V_{CC} = 5.0V$ and $T_A = +25^\circ\text{C}$

Note 8: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

| Symbol | Parameter | T _A = -40 °C to +85 °C, C _L = 50pF, R _U = R _D = 500Ω | | | | Units | Conditions (S ₂ = S ₅ = 0V) | Figure Number |
|-------------------------------------|---|---|------|------------------------|------|-------|--|------------------|
| | | V _{CC} = 4.5 – 5.5V | | V _{CC} = 4.0V | | | | |
| | | Min | Max | Min | Max | | | |
| t _{PHL} , t _{PLH} | Propagation Delay Bus-to-Bus (Note 9) | | 0.25 | | 0.25 | ns | V _I = OPEN | Figures 2, 3 |
| t _{PZH} , t _{PZL} | Output Enable Time | 1.5 | 6.5 | | 7.0 | ns | V _I = 7V for t _{PZL} V _I = OPEN for t _{PZH} | Figures 2, 3 |
| t _{PHZ} , t _{PLZ} | Output Disable Time | 1.5 | 6.7 | | 7.2 | ns | V _I = 7V for t _{PLZ} V _I = OPEN for t _{PHZ} | Figures 2, 3 |
| t _{PZH} , t _{PZL} | S _{el} (S _{0, 1}) to Output Enable Time | 1.5 | 7.0 | | 7.5 | ns | V _I = 7V for t _{PZL} V _I = OPEN for t _{PZH} | Figures 2, 3 |
| t _{PHZ} , t _{PLZ} | S _{el} (S _{0, 1}) to Output Disable Time | 1.5 | 7.5 | | 7.7 | ns | V _I = 7V for t _{PLZ} V _I = OPEN for t _{PHZ} | Figures 2, 3 |

Note 9: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

AC Electrical Characteristics: Translating Diode

| Symbol | Parameter | T _A = -40 °C to +85 °C, C _L = 50pF, R _U = R _D = 500Ω | | Units | Conditions (S ₂ = S ₅ = V _{CC}) | Figure Number |
|-------------------------------------|---|---|------|-------|--|------------------|
| | | V _{CC} = 4.5 – 5.5V | | | | |
| | | Min | Max | | | |
| t _{PHL} , t _{PLH} | Propagation Delay Bus-to-Bus (Note 10) | | 0.25 | ns | V _I = OPEN | Figures 2, 3 |
| t _{PZH} , t _{PZL} | Output Enable Time | 1.5 | 10.0 | ns | V _I = 7V for t _{PZL} V _I = OPEN for t _{PZH} | Figures 2, 3 |
| t _{PHZ} , t _{PLZ} | Output Disable Time | 1.5 | 9.0 | ns | V _I = 7V for t _{PLZ} V _I = OPEN for t _{PHZ} | Figures 2, 3 |
| t _{PZH} , t _{PZL} | S _{el} (S _{0, 1}) to Output Enable Time | 1.5 | 11.0 | ns | V _I = 7V for t _{PZL} V _I = OPEN for t _{PZH} | Figures 2, 3 |
| t _{PHZ} , t _{PLZ} | S _{el} (S _{0, 1}) to Output Disable Time | 1.5 | 10.0 | ns | V _I = 7V for t _{PLZ} V _I = OPEN for t _{PHZ} | Figures 2, 3 |

Note 10: This parameter is guaranteed by design but is not tested. This bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 11)

| Symbol | Parameter | Typ | Max | Units | Conditions |
|------------------|--------------------------------------|-----|-----|-------|--|
| C _{IN} | Control Pin Input Capacitance | 4 | | pF | V _{CC} = 5.0V, V _{IN} = 0V |
| C _{I/O} | Input/Output Capacitance "OFF State" | 8 | | pF | V _{CC} , \overline{OE} = 5.0V, V _{IN} = 0V |

Note 11: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 12)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------|----------------------------------|-----|----------------|-----|-------|-----------------------------|
| V_{OUTU} | Output Voltage During Undershoot | 2.5 | $V_{OH} - 0.3$ | | V | $S_2 = S_5 = 0V$, Figure 1 |
| | | TBD | TBD | | V | $S_2 = S_5 = V_{CC}$ |

Note 12: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

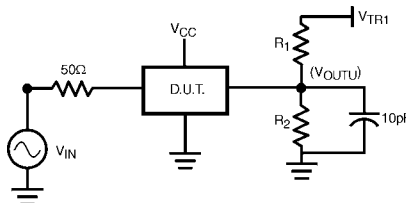
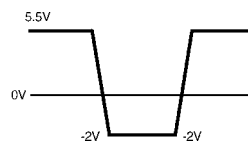


FIGURE 1.

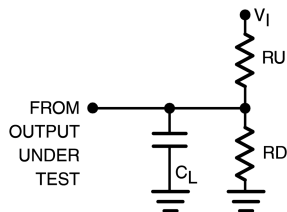
Device Test Conditions

| Parameter | Value | Units |
|-------------|--------------|----------|
| V_{IN} | see Waveform | V |
| $R_1 = R_2$ | 100K | Ω |
| V_{TRI} | 11.0 | V |
| V_{CC} | 5.5 | V |

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω
Note: C_L includes load and stray capacitance
Note: Input Frequency = 1.0 MHz, $t_W = 500$ ns

FIGURE 2. AC Test Circuit

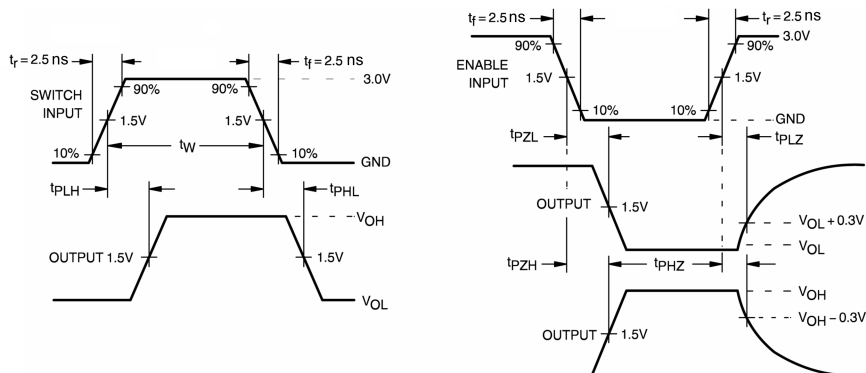


FIGURE 3. AC Waveforms

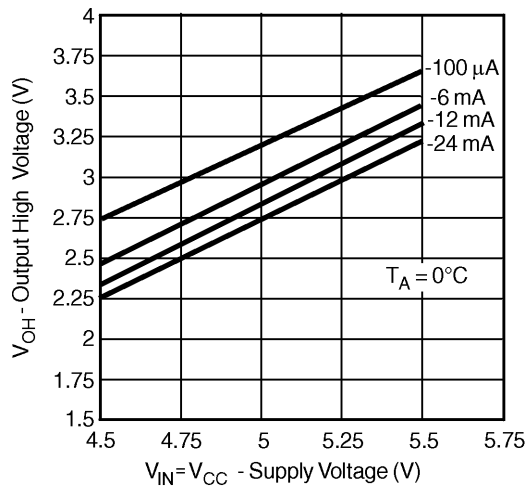
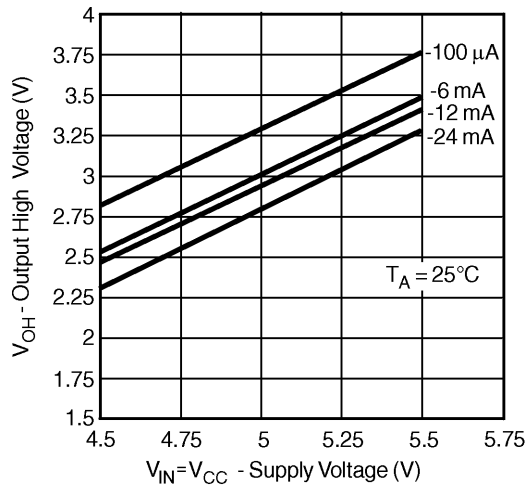
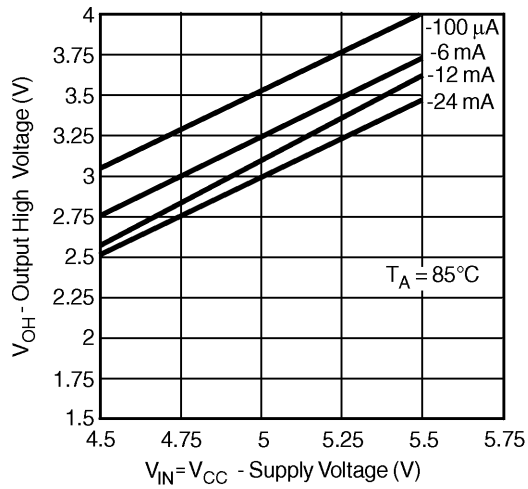
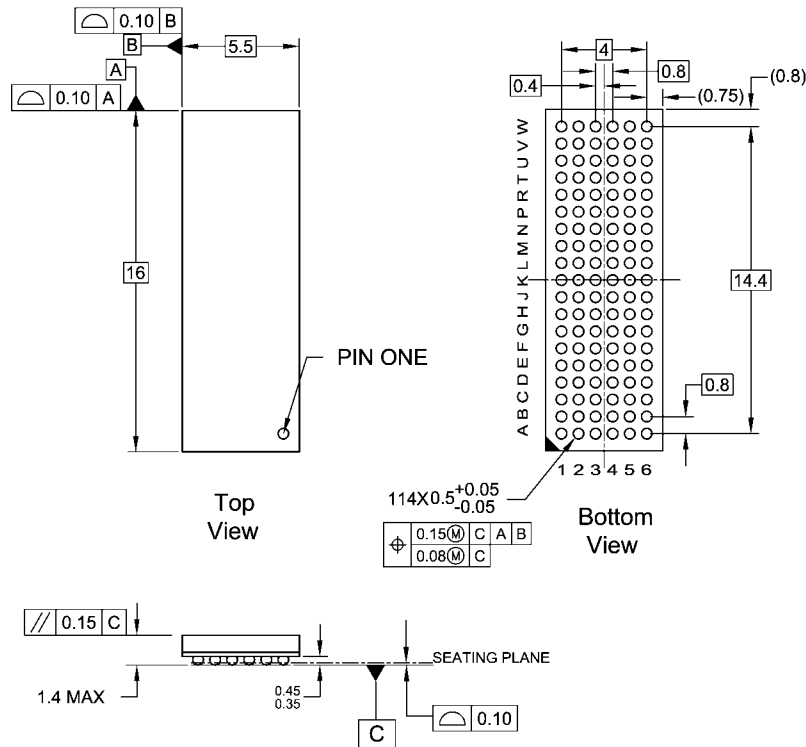


FIGURE 4.

Physical Dimensions inches (millimeters) unless otherwise noted



- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
 - B. ALL DIMENSIONS IN MILLIMETERS
 - C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
 - D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

**114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A**

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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