# LF48212
## 12 x 12-bit Alpha Mixer

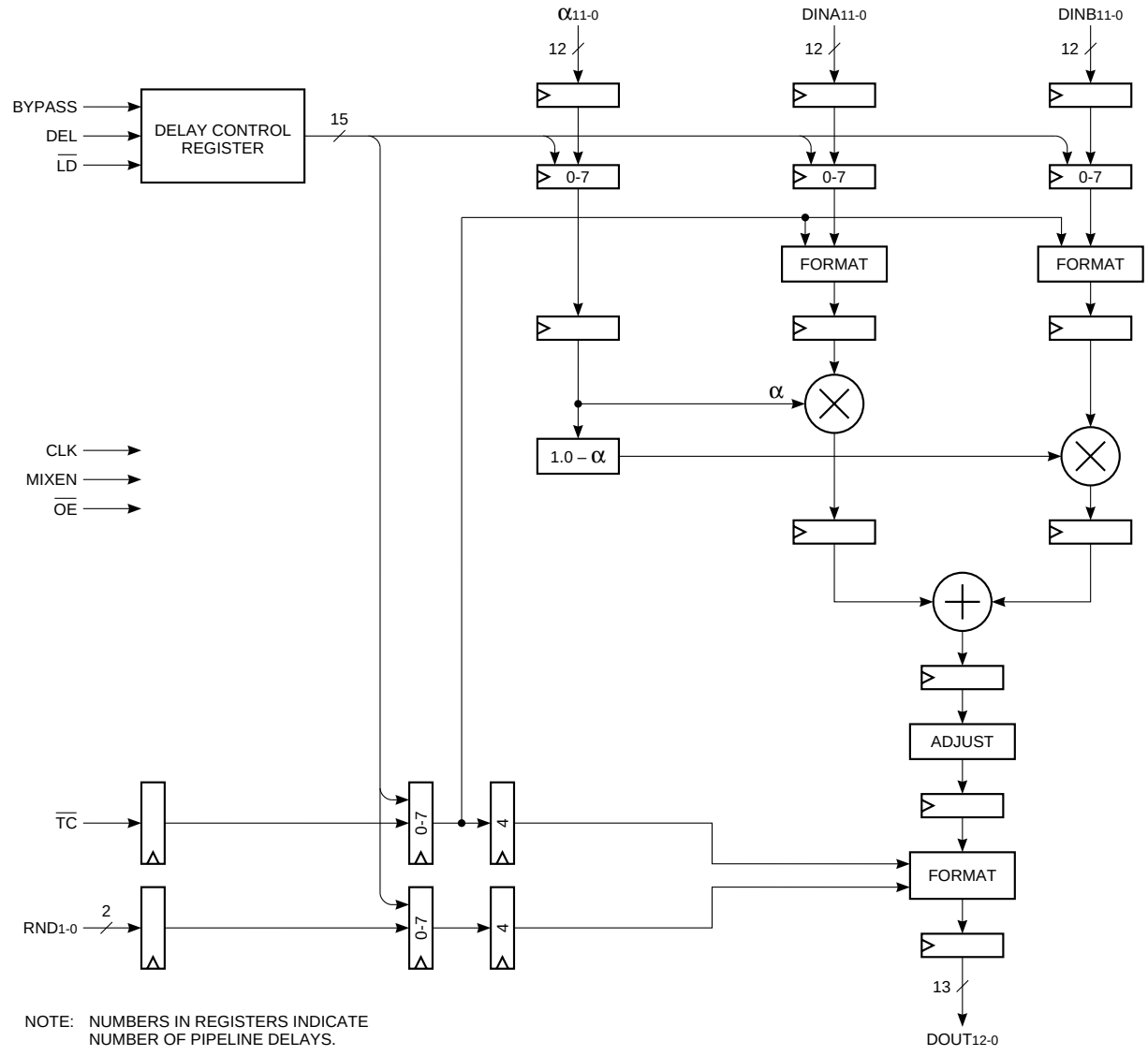
## FEATURES

- 50 MHz Data and Computation Rate
- Two's Complement or Unsigned Operands
- On-board Programmable Delay Stages
- Programmable Output Rounding
- Replaces Harris HSP48212
- Package Styles Available:
  - 68-pin PLCC, J-Lead
  - 64-pin PQFP

## DESCRIPTION

The LF48212 is a high-speed video alpha mixer capable of mixing video signals at real-time video rates. It takes two 12-bit video signals and mixes them together using an alpha mix factor. Alpha determines the weighting that each video signal receives during the mix operation. The input video data can be in either unsigned or two's complement format, but both inputs must be in the same format. Independently controlled programmable delay stages are provided for the input and control signals to allow for allignment of input data if necessary. The delay stages can be programmed to have from 0 to 7 delays. The 13-bit output of the alpha mixer is registered with three-state drivers and may be rounded to 8, 10, 12, or 13-bits.

## LF48212 Block Diagram




NOTE: NUMBERS IN REGISTERS INDICATE NUMBER OF PIPELINE DELAYS.

## SIGNAL DEFINITIONS

### Power

*$V_{CC}$ and GND*

+5 V power supply. All pins must be connected.

### Clock

*CLK — Master Clock*

The rising edge of CLK strobes all enabled registers except for the Delay Control Register.

### Inputs

*DINA11-0 — Pixel Data Input A*

DINA11-0 is one of the 12-bit registered data input ports. Data is latched on the rising edge of CLK.

*DINB11-0 — Pixel Data Input B*

DINB11-0 is the other 12-bit registered data input port. Data is latched on the rising edge of CLK.

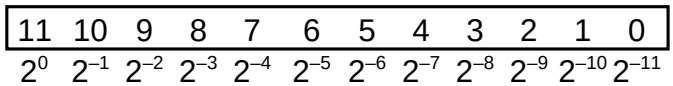
*$\alpha_{11-0}$ — Alpha Mix Input*

$\alpha_{11-0}$ determines the weighting applied to the data input signals before being mixed together. DINA11-0 and DINB11-0 receive weightings of $\alpha$ and $1.0 - \alpha$ respectively. $\alpha_{11-0}$ is unsigned and restricted to the range of 0 to 1.0. Figure 1 shows the data format for $\alpha_{11-0}$. If a value greater than 1.0 is latched into the Alpha Mix Input, internal circuitry will force the value to be equal to 1.0. Data is latched on the rising edge of CLK.

*DEL — Delay Data Input*

DEL is used to load the Delay Control Register. The Delay Control Register contains a 15-bit value which determines the number of delay stages added to the input and control signals. The 15-bit data value is loaded serially into the Delay Control Register using DEL and $\overline{LD}$. Data present on DEL is latched on the rising edge of $\overline{LD}$.

**FIGURE 1. ALPHA MIX INPUT FORMAT**




### Outputs

*DOUT12-0 — Data Output*

DOUT12-0 is the 13-bit registered data output port.

### Controls

*$\overline{TC}$ — Data Format Control*

$\overline{TC}$ determines if the input data is in unsigned or two's complement format. If $\overline{TC}$ is LOW, the data is in two's complement format. If $\overline{TC}$ is HIGH, the data is in unsigned format. Data present on $\overline{TC}$ is latched on the rising edge of CLK. $\overline{TC}$ only affects the data that is being latched into the LF48212. Changing $\overline{TC}$ does not affect internal data already in the pipeline.

*MIXEN — Alpha Mix Input Enable*

When HIGH, data on $\alpha_{11-0}$ is latched into the LF48212 on the rising edge of CLK. When LOW, data on $\alpha_{11-0}$ is not latched and the last value loaded is held as the alpha mix value.

*$\overline{LD}$ — Load Strobe*

The rising edge of $\overline{LD}$ latches the data on DEL into the Delay Control Register.

*BYPASS — Bypass Delay Stage Control*

The BYPASS control is used to bypass the internal programmable delay stages. When BYPASS is set HIGH, the Delay Control Register will automatically be loaded with a "0". This will set the number of programmable delay stages to zero for all input and control signals. When BYPASS is LOW, the desired number of delay stages can be set by loading the Delay Control Register with the appropriate value. Note that this signal is not intended to change during active operation of the LF48212.

*RND1-0 — Output Rounding Control*

RND1-0 determines how the output of the LF48212 is rounded. The output may be rounded to 8, 10, 12, or 13-bits. Table 1 lists the different rounding possibilities and the associated value for RND1-0. Rounding is accomplished by adding a "1" to the bit to the right of what will become the least significant bit. Then the bit that had the "1" added to it and all bits to the right of it are set to "0". Data present on RND1-0 is latched on the rising edge of CLK. When RND1-0 is latched in, it only applies to the video input data latched in at the same time. Changing RND1-0 does not affect the rounding format for internal data already in the pipeline.

*$\overline{OE}$ — Output Enable*

When $\overline{OE}$ is LOW, DOUT12-0 is enabled for output. When $\overline{OE}$ is HIGH, DOUT12-0 is placed in a high-impedance state.

**TABLE 1. OUTPUT ROUNDING**

| RND1-0 | ROUNDING FORMAT |
|---|---|
| 00 | Round to 8-bits |
| 01 | Round to 10-bits |
| 10 | Round to 12-bits |
| 11 | Round to 13-bits |

## FUNCTIONAL DESCRIPTION

The two video signals to be mixed together are input to the LF48212 using DINA11-0 and DINB11-0. Data present on DINA11-0 and DINB11-0 is latched on the rising edge of CLK. The input data may be in either unsigned or two's complement format, but both inputs must be in the same format. $\overline{TC}$ determines the format of the input data. When $\overline{TC}$ is HIGH, the input data is in unsigned format. When $\overline{TC}$ is LOW, the input data is in two's complement format. $\overline{TC}$ is latched on the rising edge of CLK and only affects the input data latched in at the same time. The data already in the pipeline is not affected when $\overline{TC}$ changes.

DINA11-0 and DINB11-0 are mixed together using an alpha mix factor ($\alpha_{11\text{-}0}$) as defined by the equation listed in Figure 2. $\alpha_{11\text{-}0}$ is unsigned and restricted to the range of 0 to 1.0. MIXEN controls the loading of alpha mix data. When MIXEN is HIGH, data present on $\alpha_{11\text{-}0}$ is latched on the rising edge of CLK. When MIXEN is LOW, data present on $\alpha_{11\text{-}0}$ is not latched and the last value loaded is held as the alpha mix value.

It is possible to add extra delay stages to the input data and control signals by using the programmable delay stages. The 15-bit value (DELAY14-0) stored in the Delay Control Register determines the number of delay stages added. DELAY14-0 is divided into 5 groups of 3-bits each. Each 3-bit group contains the delay information for one of the input data or control signals. Figure 3 shows the block diagram of the Delay Control Register as well as a list of the input data and control signals that may be delayed and the DELAY signals that control them. The delay length can be programmed to be from 0 to 7 stages. The delay length is set by loading the binary equivalent of the desired delay length into the appropriate 3-bit group. For example, to add four extra delay stages to DINB11-0, DELAY5-3 should be set to "100". DELAY14-0 is loaded serially into the Delay Control Register using DEL and $\overline{LD}$. DELAY0 is the first value loaded and DELAY14 is the last. Data present on DEL is latched on the rising edge of $\overline{LD}$. BYPASS is used to disable the programmable delay stages. When BYPASS is HIGH, the Delay Control Register is automatically loaded with a "0". This sets all programmable delay stages to a length of zero. When BYPASS is LOW, the Delay Control Register may be loaded to set the desired number of delay stages. Note that BYPASS is not intended to change during active operation of the LF48212.

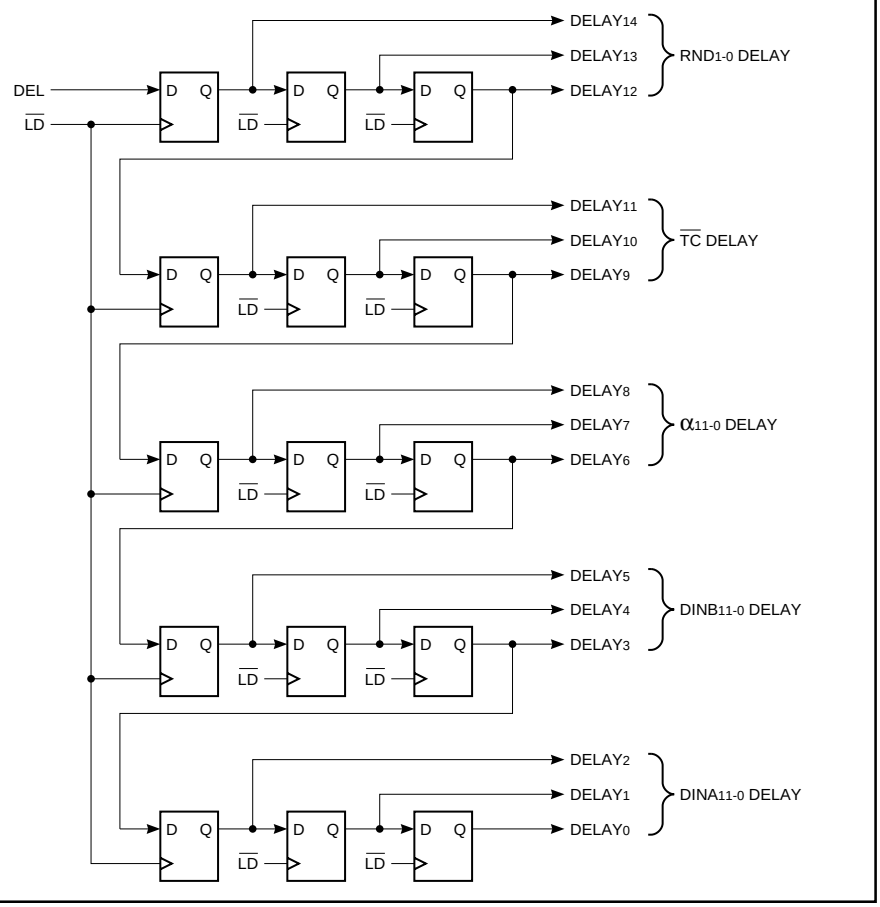
The Adjust stage of the LF48212 is used to maximize the precision of the output data. Since $\alpha$ can never be larger than 1.0, the most significant bit of the internal summer output is not needed. The Adjust stage takes the output of the internal summer and left shifts the data one bit position. This removes the MSB of the internal summer output and provides one more bit of precision for the output data.

The output data of the LF48212 may be rounded to 8, 10, 12, or 13-bits. RND1-0 determines how the output is rounded (See Table 1). RND1-0 is latched on the rising edge of CLK and only affects the input data latched in at the same time. The data already in the pipeline is not affected when RND1-0 changes.

**FIGURE 2. OUTPUT EQUATION**

$$OUTPUT = \alpha(DINA) + (1 - \alpha)DINB$$

**FIGURE 3. DELAY CONTROL REGISTER BLOCK DIAGRAM**



## MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
**V**CC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

## OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

| **Mode** | **Temperature Range** (Ambient) | **Supply Voltage** |
|---|---|---|
| Active Operation, Commercial | 0°C to +70°C | 4.75 V ≤ **V**CC ≤ 5.25 V |

## ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

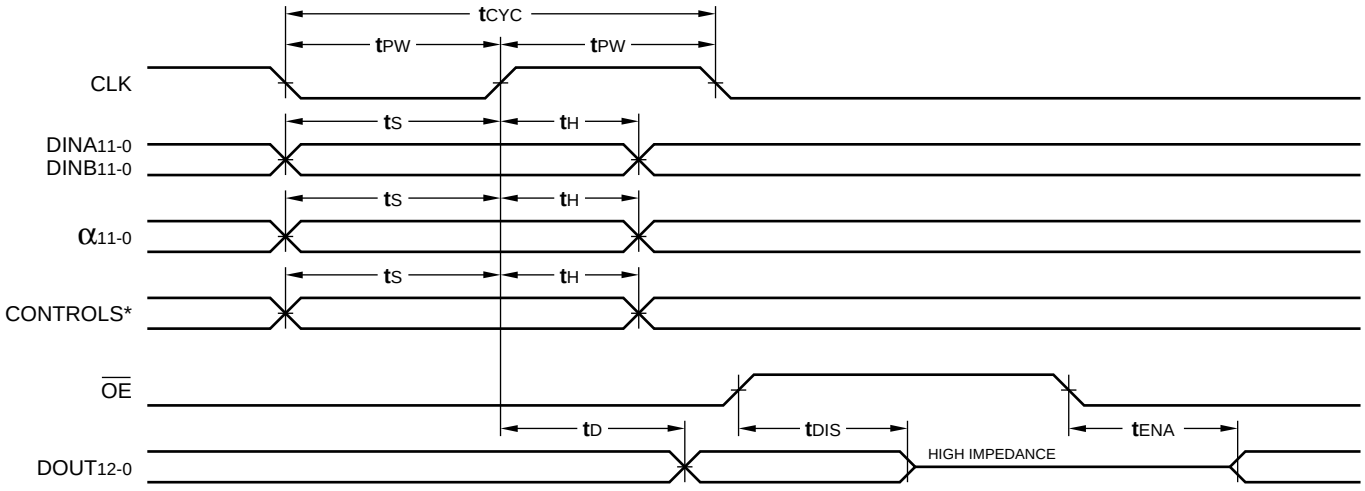
| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **V**OH | Output High Voltage | **V**CC = Min., **I**OH = –400 µA | 2.6 | | | V |
| **V**OL | Output Low Voltage | **V**CC = Min., **I**OL = 2.0 mA | | | 0.4 | V |
| **V**IH | Input High Voltage | | 2.0 | | **V**CC | V |
| **V**IL | Input Low Voltage | (Note 3) | 0.0 | | 0.8 | V |
| **I**IX | Input Current | Ground ≤ **V**IN ≤ **V**CC (Note 12) | | | ±10 | µA |
| **I**OZ | Output Leakage Current | Ground ≤ **V**OUT ≤ **V**CC (Note 12) | | | ±10 | µA |
| **I**CC1 | **V**CC Current, Dynamic | (Notes 5, 6) | | | 120 | mA |
| **I**CC2 | **V**CC Current, Quiescent | (Note 7) | | | 500 | µA |
| **C**IN | Input Capacitance | **T**A = 25°C, f = 1 MHz | | | 10 | pF |
| **C**OUT | Output Capacitance | **T**A = 25°C, f = 1 MHz | | | 10 | pF |

## SWITCHING CHARACTERISTICS

### COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

| Symbol | Parameter | LF48212– 25 Min | LF48212– 25 Max | LF48212– 20 Min | LF48212– 20 Max |
|---|---|---|---|---|---|
| $t_{CYC}$ | Cycle Time | 25 | | 20 | |
| $t_{PW}$ | Clock Pulse Width | 10 | | 10 | |
| $t_S$ | Input Setup Time | 11 | | 11 | |
| $t_H$ | Input Hold Time | 0 | | 0 | |
| $t_D$ | Output Delay | | 14 | | 14 |
| $t_{ENA}$ | Three-State Output Enable Delay (Note 11) | | 13 | | 13 |
| $t_{DIS}$ | Three-State Output Disable Delay (Note 11) | | 13 | | 13 |

### SWITCHING WAVEFORMS: DATA I/O

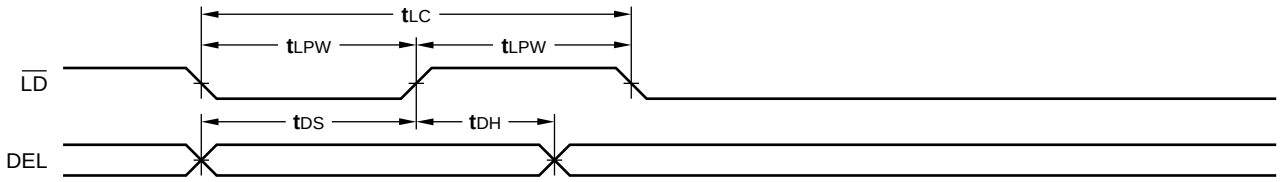



*includes MIXEN, $\overline{TC}$, and $RND_{1\text{-}0}$.

## COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

| Symbol | Parameter | LF48212– 25 Min | 25 Max | 20 Min | 20 Max |
|---|---|---|---|---|---|
| $t_{LC}$ | LD Cycle Time | 25 | | 20 | |
| $t_{LPW}$ | LD Pulse Width | 10 | | 10 | |
| $t_{DS}$ | DEL Setup Time | 12 | | 12 | |
| $t_{DH}$ | DEL Hold Time | 0 | | 0 | |

## SWITCHING WAVEFORMS: DELAY CONTROL REGISTER DATA



## NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above **V**CC will be clamped beginning at –0.6 V and **V**CC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 40 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except **t**DIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and **V**CC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the **t**ENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the **t**DIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

**FIGURE A. OUTPUT LOADING CIRCUIT**

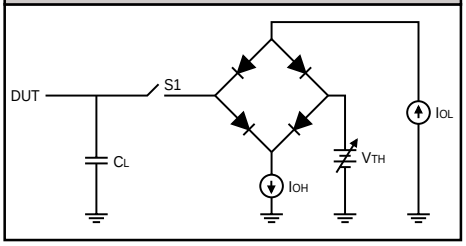
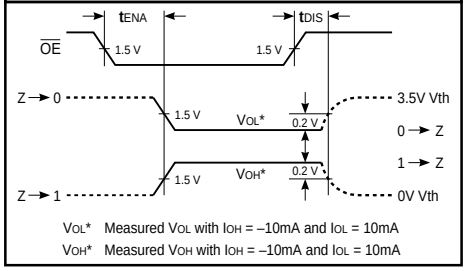
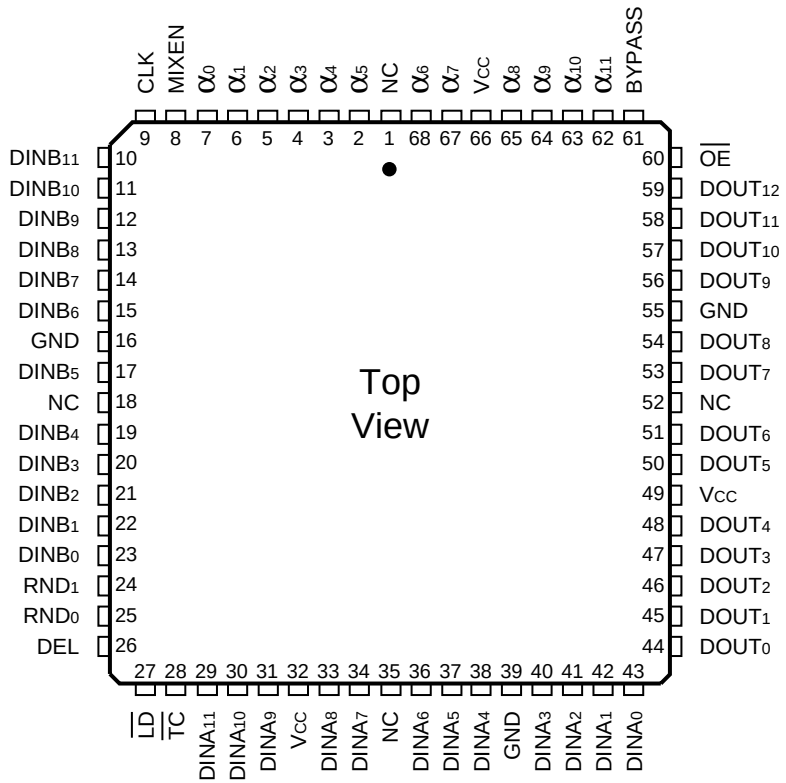



**FIGURE B. THRESHOLD LEVELS**



## ORDERING INFORMATION

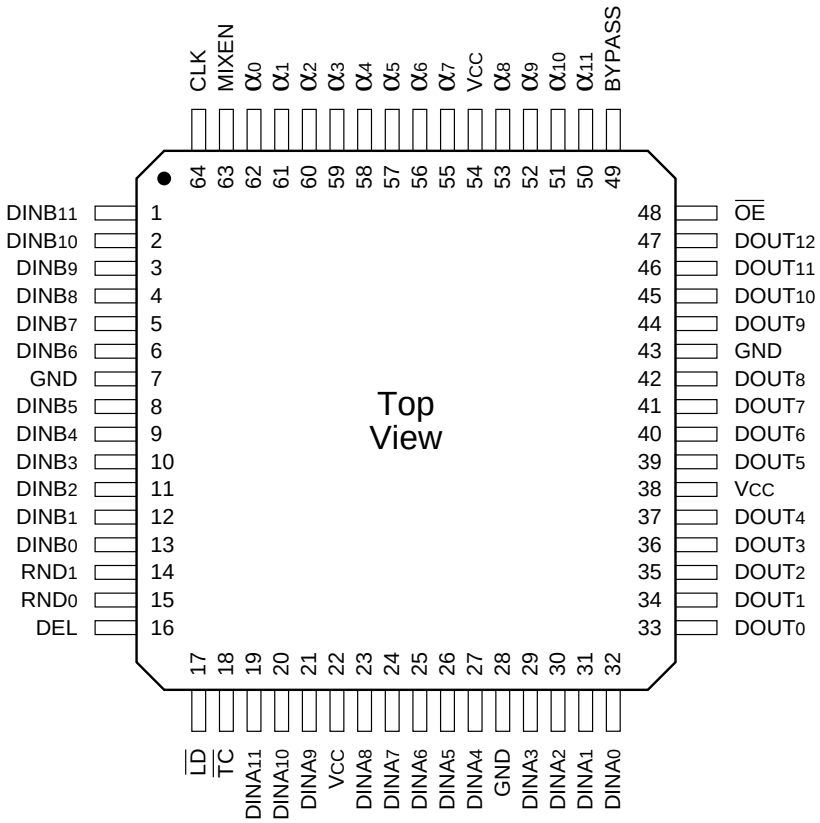
**68-pin**




| Speed | Plastic J-Lead Chip Carrier (J2) |
|---|---|
| | **0°C to +70°C — COMMERCIAL SCREENING** |
| 25 ns | LF48212JC25 |
| 20 ns | LF48212JC20 |

## ORDERING INFORMATION

**64-pin**




| Speed | Plastic Quad Flatpack (Q3) |
|---|---|
| | **0°C to +70°C — COMMERCIAL SCREENING** |
| 25 ns | LF48212QC25 |
| 20 ns | LF48212QC20 |