

PRELIMINARY
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 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS 38C2 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 38C2 group is the 8-bit microcomputer based on the 740 family core technology.

The 38C2 group has an LCD drive control circuit, a 10-channel A-D converter, and a Serial I/O as additional functions.

The various microcomputers in the 38C2 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time 0.25 μ s
 (at 8MHz oscillation frequency)
- Memory size
 ROM 16 K to 60 K bytes
 RAM 640 to 2048 bytes
- Programmable input/output ports 51
 (common to SEG: 24)
- Interrupts 18 sources, 16 vectors
- Timers 8-bit X 4, 16-bit X 2
- A-D converter 10-bit X 8 channels
- Serial I/O 8-bit X 2 (UART or Clock-synchronized)
- PWM 10-bit X 2, 16-bit X 1 (common to IGBT output)

- LCD drive control circuit
 Bias 1/2, 1/3
 Duty 1/2, 1/3, 1/4
 Common output 4
 Segment output 24
- Two clock generating circuits
 (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer 8-bit X 1
- LED direct drive port 8
 (average current: 15 mA, peak current: 30 mA, total current: 90 mA)
- Power source voltage
 In through mode 4.0 to 5.5 V
 (at 8 MHz oscillation frequency)
 In frequency/2 mode 1.8 to 5.5 V
 (at 4 MHz oscillation frequency, A-D operation excluded)
 In low-speed mode 1.8 to 5.5 V
 (at 32 kHz oscillation frequency)
- Power dissipation
 In through mode 26 mW
 (at 8 MHz oscillation frequency, Vcc = 5 V)
 In low-speed mode 21 μ W
 (at 32 kHz oscillation frequency, Vcc = 3 V)
- Operating temperature range - 20 to 85°C

PIN CONFIGURATION (TOP VIEW)

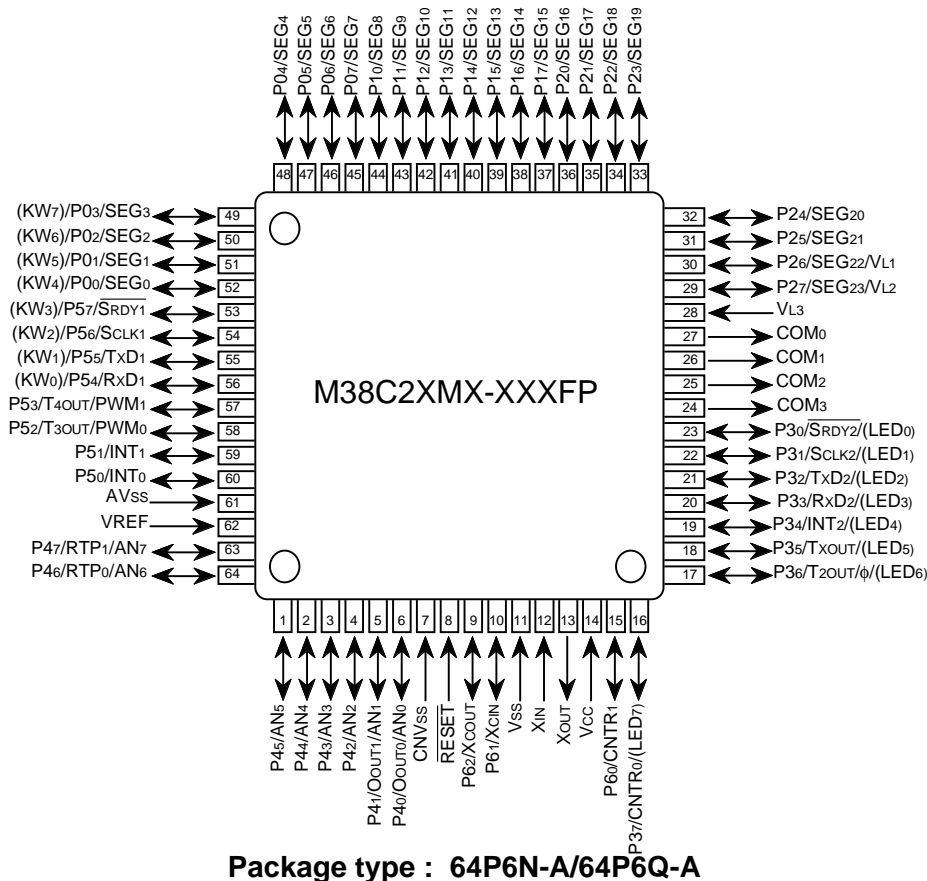


Fig. 1 M38C2XXM-XXXXFP pin configuration

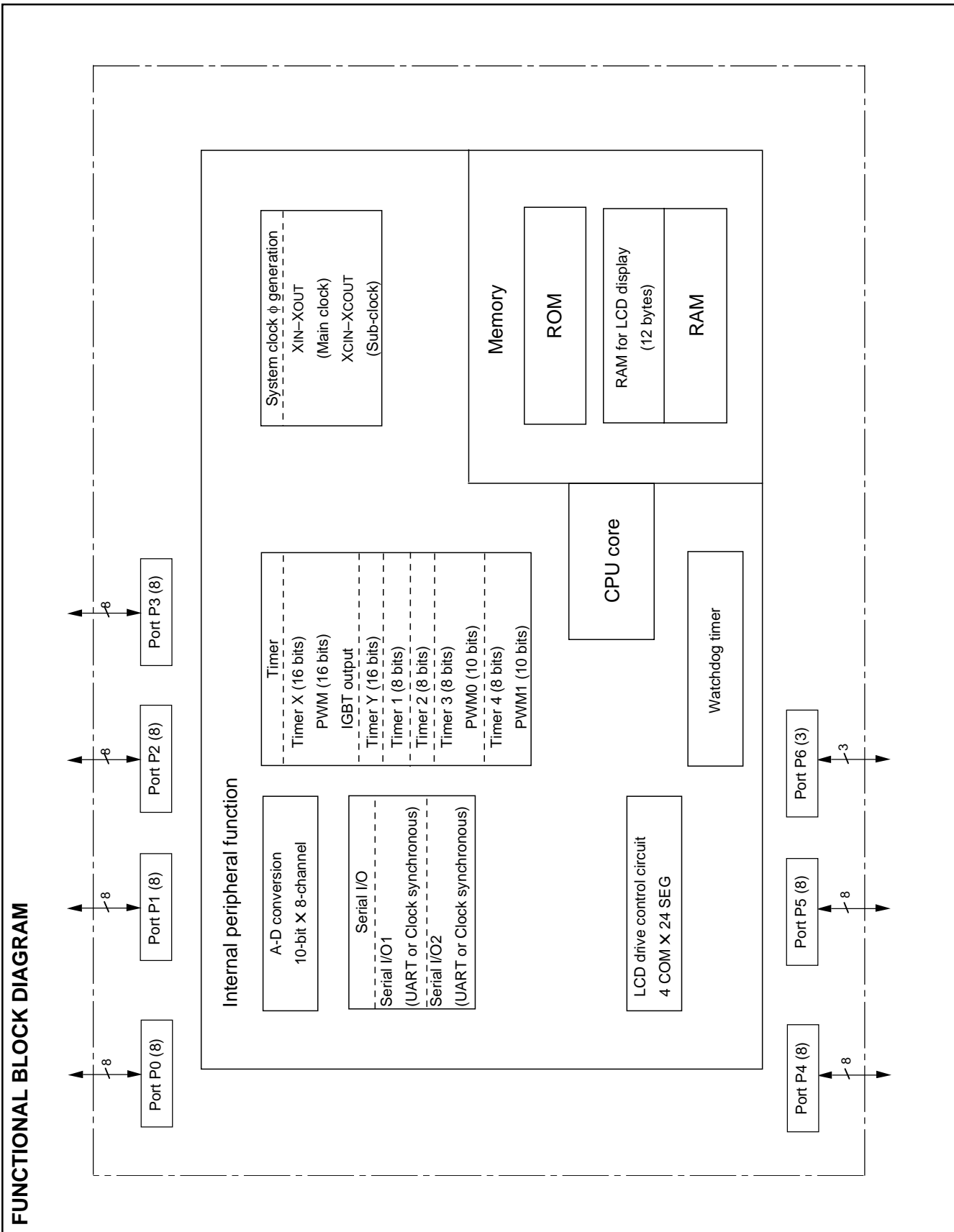


Fig. 2 Functional block diagram

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PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function	
VCC, VSS	Power source	• Apply voltage of 1.8 V to 5.5 V to VCC, and 0 V to VSS.		
VREF	Analog reference voltage	• Reference voltage input pin for A-D converter.		
AVSS	Analog power source	• GND input pin for A-D converter. Connect to VSS.		
RESET	Reset input	• Reset input pin for active "L."		
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between XIN pin and XOUT pin.		
XOUT	Clock output	• Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. When an external clock is used, connect the clock source to XIN, and leave XOUT pin open.		
VL3	LCD power source	• Input $0 \leq VL1 \leq VL2 \leq VL3 \leq VCC$ voltage. • Input 0 – VL3 voltage to LCD.		
COM0 – COM3	Common output	• LCD common output pins. • COM2 and COM3 are not used at 1/2 duty ratio. • COM3 is not used at 1/3 duty ratio.		
P00/SEG0 – P03/SEG3	I/O port P0	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each port to be individually programmed as either input or output. • Pull-up control is enabled.	• LCD segment output pins	• Key input interrupt pins
P04/SEG4 – P07/SEG7				
P10/SEG8 – P17/SEG15				
P20/SEG16 – P25/SEG21	I/O port P2			• LCD power source input pins
P26/SEG22/VL1 P27/SEG23/VL2				
P30/SRDY2 P31/SCLK2 P32/TxD2 P33/RxD2	I/O port P3			• Serial I/O2 function pins
P34/INT2				
P35/TXOUT P36/T2OUT/φ P37/CNTR0				
P40/OOUT0/AN0 P41/OOUT1/AN1				
P42/AN2 – P45/AN5	I/O port P4			• AD converter input pins
P46/RTP0/AN6 P47/RTP1/AN7				
P50/INT0 P51/INT1	I/O port P5			• Oscillation external output pins
P52/T3OUT/PWM0 P53/T4OUT/PWM1				
P54/RxD1 P55/TxD1 P56/SCLK1 P57/SRDY1				
				• Real time port function pins
				• External interrupt pins
				• Timer 3, Timer 4 output pins • PWM output pins
				• Serial I/O1 function pins • Key input interrupt input pins

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PIN DESCRIPTION

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
P60/CNTR1	I/O port P6	<ul style="list-style-type: none">• 3-bit I/O port.• CMOS compatible input level.• CMOS 3-state output structure.• I/O direction register allows each pin to be individually programmed as either input or output.• Pull-up control is enabled.	<ul style="list-style-type: none">• Timer Y function pin
P61/XCIN			<ul style="list-style-type: none">• I/O pins for sub-clock generating circuit. Connect oscillators to them.
P62/XCOUT			
CNVSS	CNVSS	<ul style="list-style-type: none">• VPP power input pin in the flash mode. When MCU is operating, connect to VSS.	

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PART NUMBERING

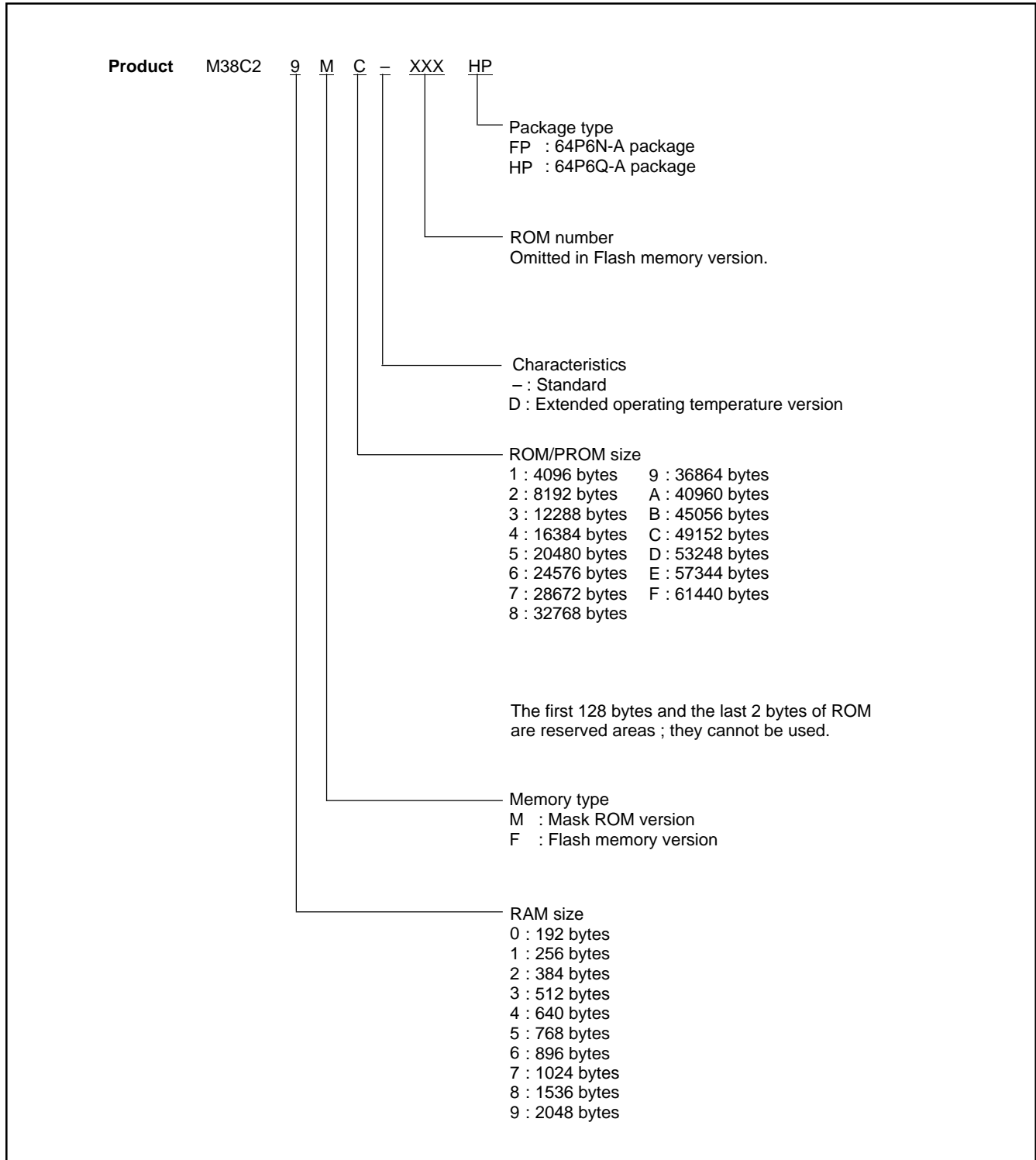


Fig. 3 Part numbering

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GROUP EXPANSION

Mitsubishi plans to expand the 38C2 group as follows.

Packages

64P6Q-A 0.5 mm-pitch plastic molded QFP
 64P6N-A 0.8 mm-pitch plastic molded QFP

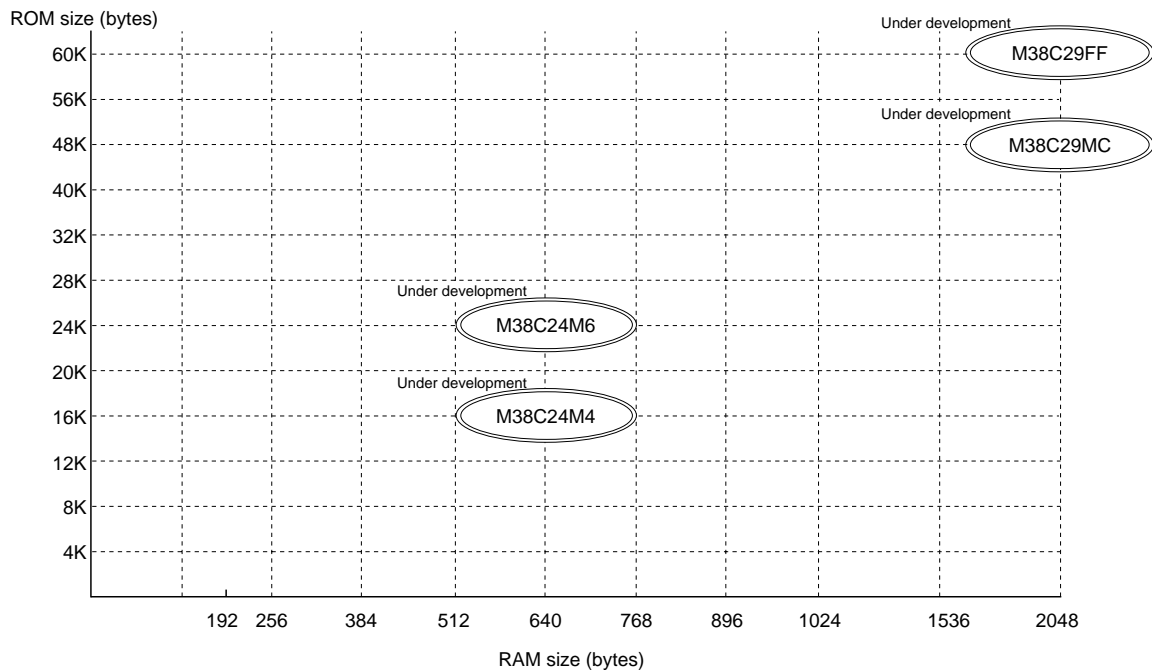
Memory Type

Support for mask ROM, Flash-memory versions

Memory Size

ROM/flash memory size 16 K to 60 K bytes
 RAM size 640 to 2048 bytes

Memory Expansion Plan



Products under development or planning : the development schedule and specification may be revised without notice.

Fig. 4 Memory expansion plan

Currently supported products are listed below.

Table 3 Support products

As of May 2000

Product name	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38C29MC-XXXFP	49152 (49022)	2048	64P6N-A	Mask ROM version
M38C29MC-XXXHP			64P6Q-A	Mask ROM version
M38C24M6-XXXFP	24576 (24446)	640	64P6N-A	Mask ROM version
M38C24M6-XXXHP			64P6Q-A	Mask ROM version
M38C24M4-XXXFP	16384 (16254)	640	64P6N-A	Mask ROM version
M38C24M4-XXXHP			64P6Q-A	Mask ROM version
M38C29FFFP	61440 (61310)	2048	64P6N-A	Flash memory version
M38C29FFHP			64P6Q-A	Flash memory version

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FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 38C2 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

- The FST and SLW instructions cannot be used.
- The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

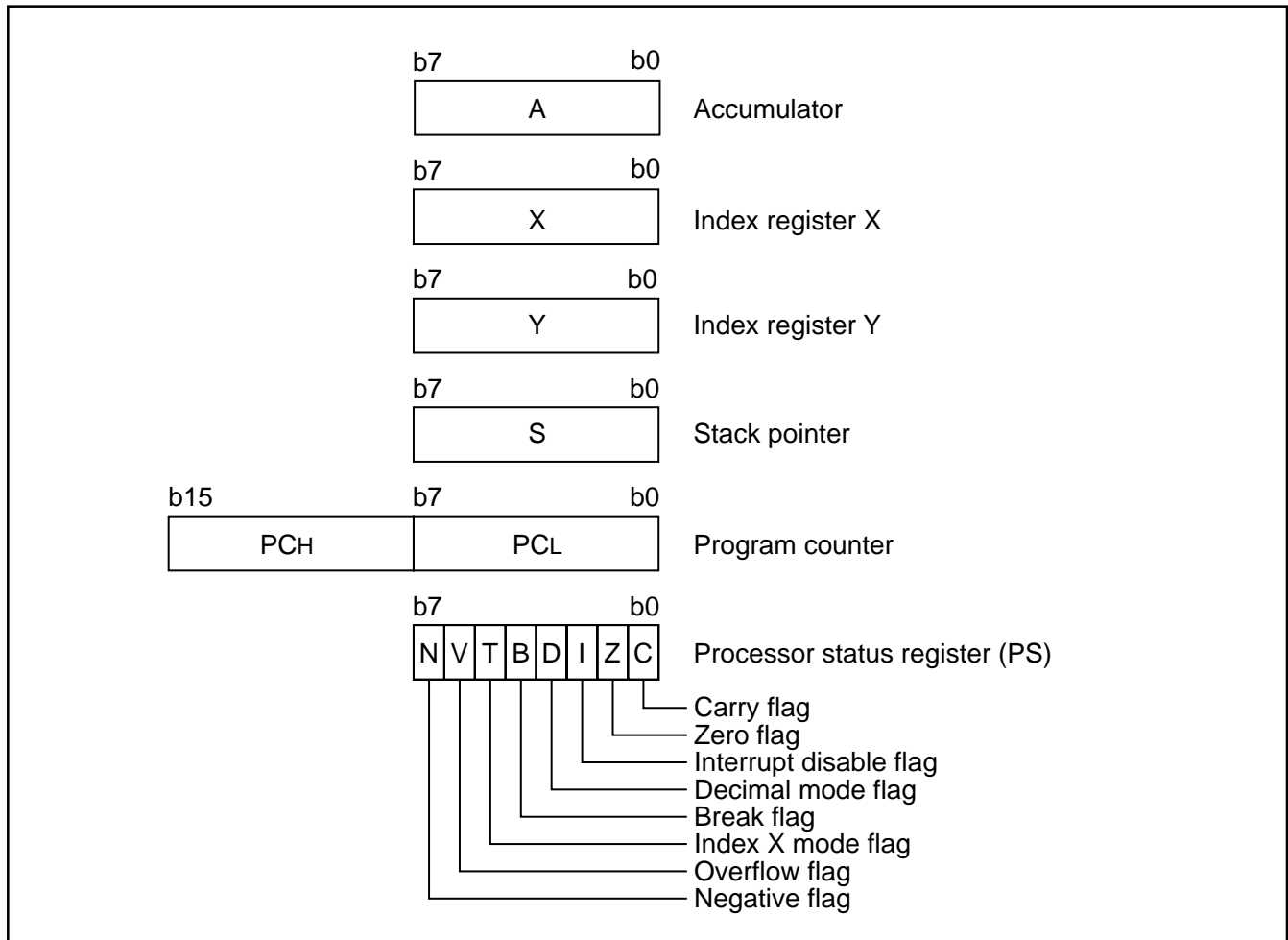
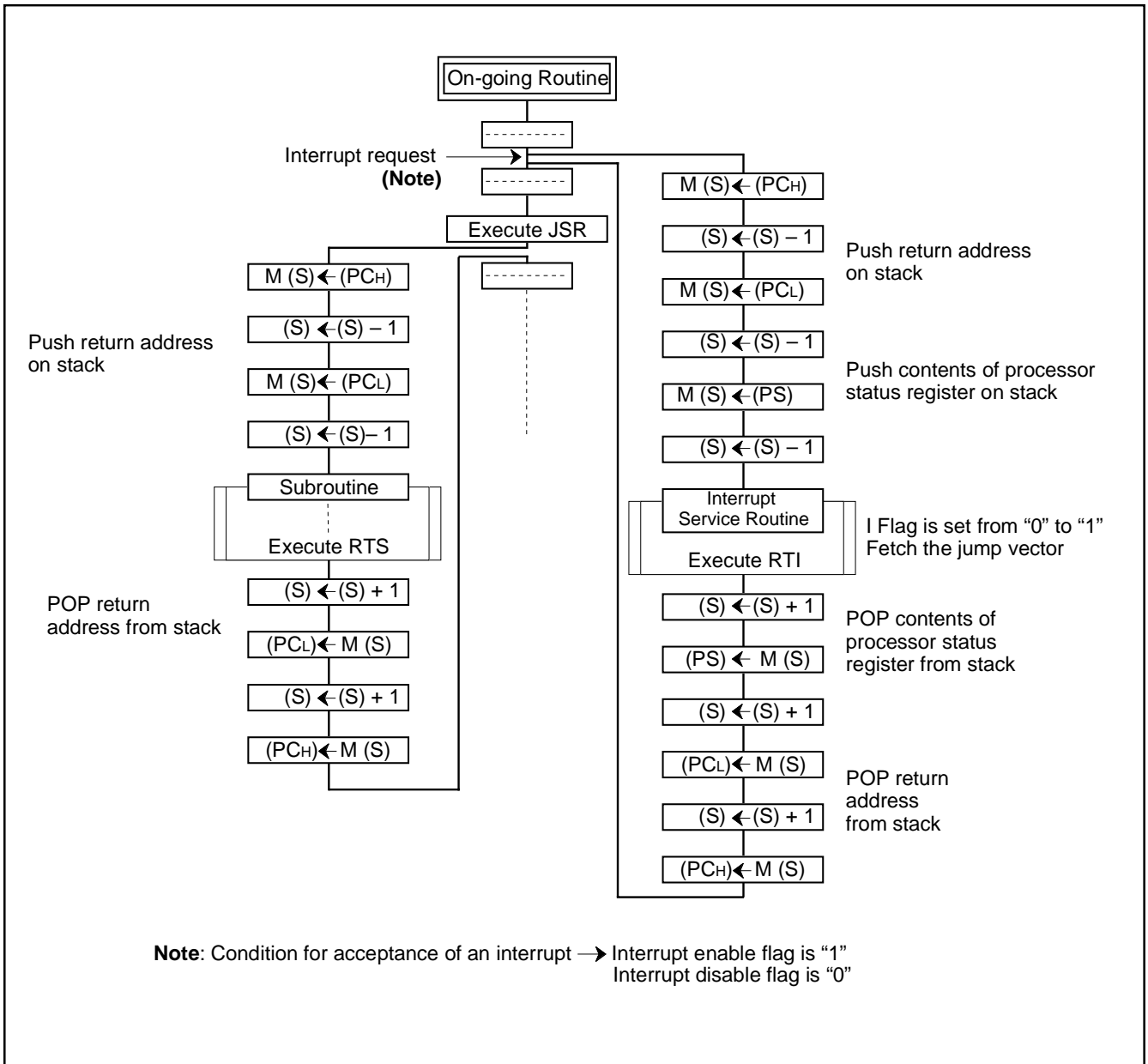


Fig. 5 740 Family CPU register structure



Note: Condition for acceptance of an interrupt → Interrupt enable flag is "1"
 Interrupt disable flag is "0"

Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

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[Processor Status Register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)
 The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
- Bit 1: Zero flag (Z)
 The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".
- Bit 2: Interrupt disable flag (I)
 The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
 Interrupts are disabled when the I flag is "1".
- Bit 3: Decimal mode flag (D)
 The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".
 Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

- Bit 4: Break flag (B)
 The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".
- Bit 5: Index X mode flag (T)
 When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.
- Bit 6: Overflow flag (V)
 The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.
- Bit 7: Negative flag (N)
 The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B₁₆

The CPU mode register contains the stack page selection bit and the control bit for the internal system clock.

The CPU mode register is allocated at address 003B₁₆.

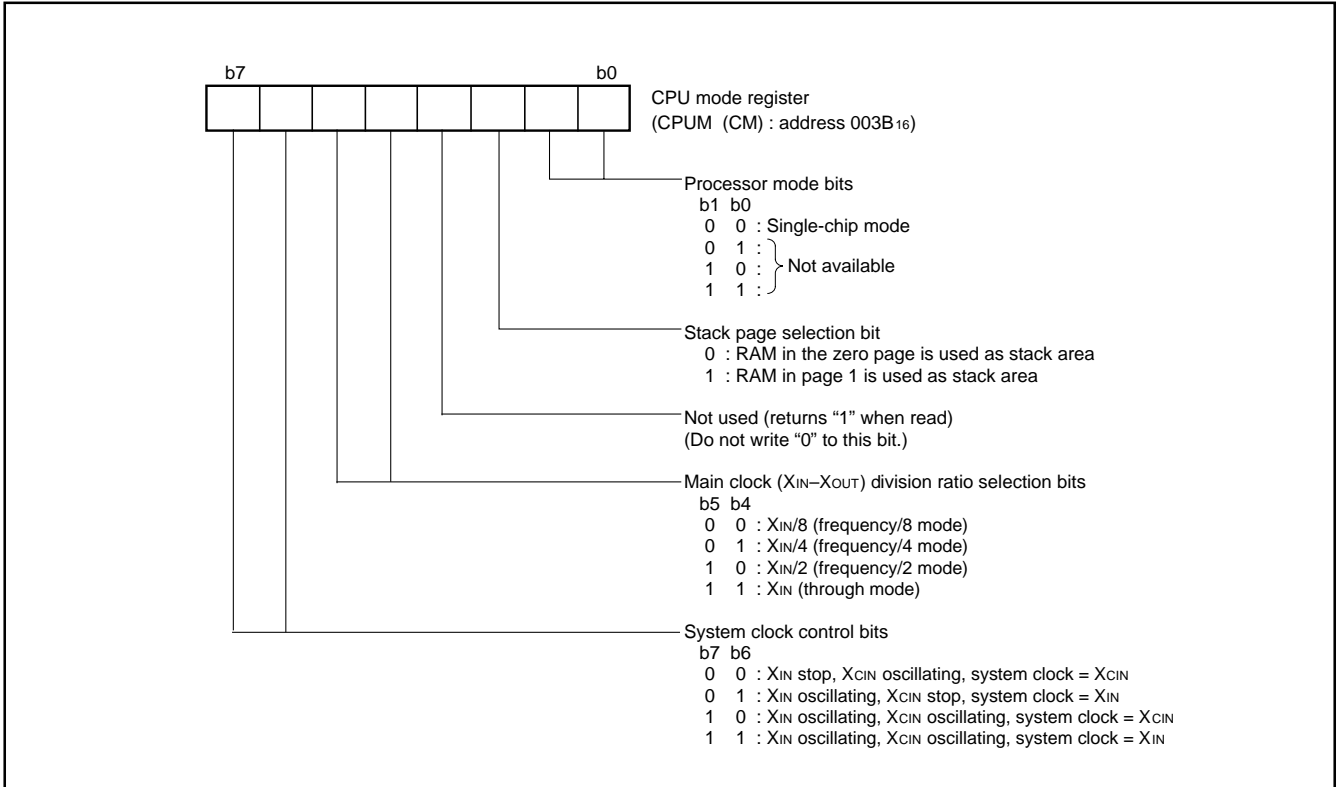


Fig. 7 Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

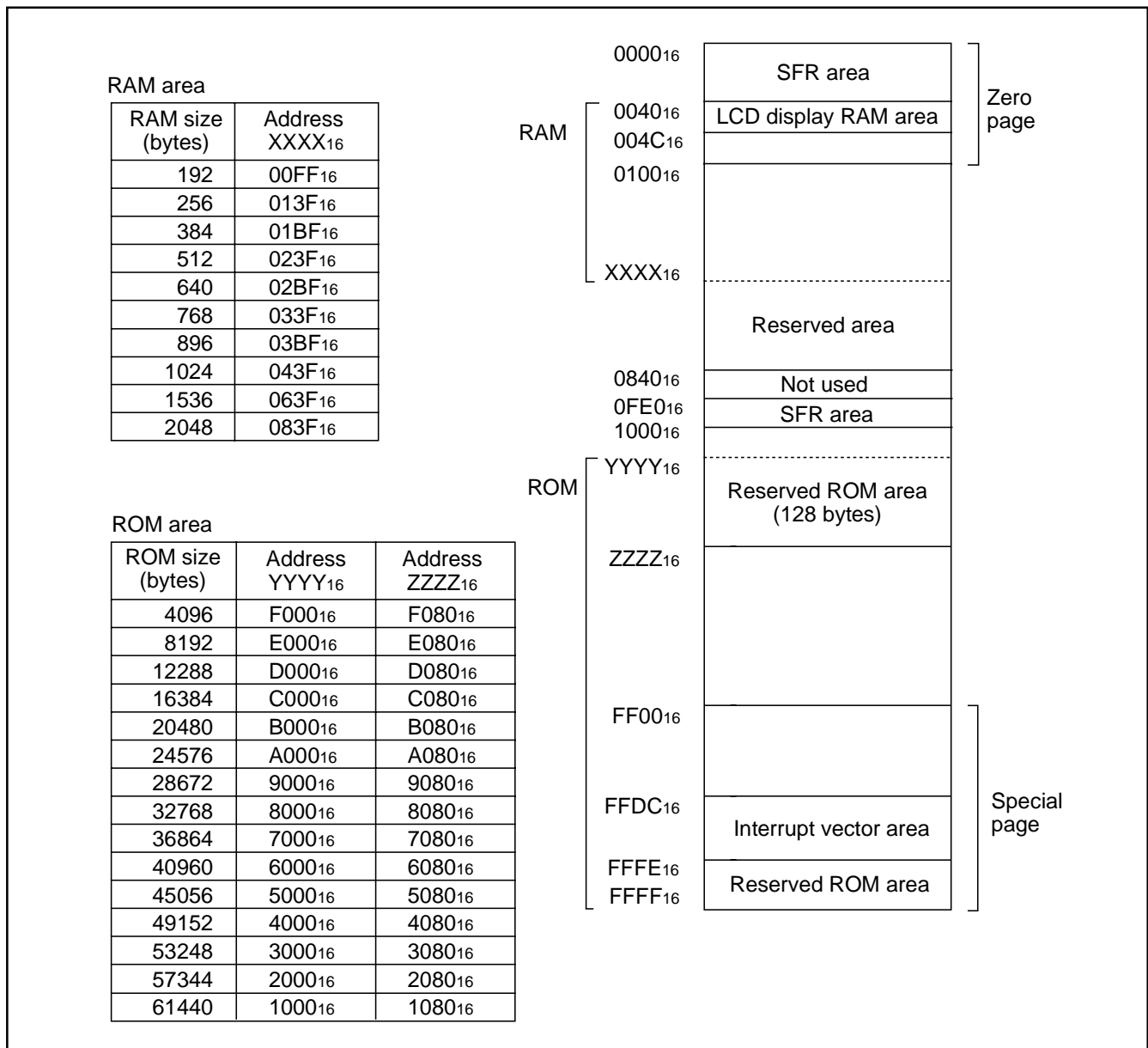


Fig. 8 Memory map diagram

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0000 ¹⁶	Port P0 (P0)	0020 ¹⁶	Timer 1 (T1)
0001 ¹⁶	Port P0 direction register (P0D)	0021 ¹⁶	Timer 2 (T2)
0002 ¹⁶	Port P1 (P1)	0022 ¹⁶	Timer 3 (T3)
0003 ¹⁶	Port P1 direction register (P1D)	0023 ¹⁶	Timer 4 (T4)
0004 ¹⁶	Port P2 (P2)	0024 ¹⁶	PWM01 register (PWM01)
0005 ¹⁶	Port P2 direction register (P2D)	0025 ¹⁶	Timer 12 mode register (T12M)
0006 ¹⁶	Port P3 (P3)	0026 ¹⁶	Timer 34 mode register (T34M)
0007 ¹⁶	Port P3 direction register (P3D)	0027 ¹⁶	
0008 ¹⁶	Port P4 (P4)	0028 ¹⁶	Compare register (low-order) (COMPL)
0009 ¹⁶	Port P4 direction register (P4D)	0029 ¹⁶	Compare register (high-order) (COMPH)
000A ¹⁶	Port P5 (P5)	002A ¹⁶	Timer X (low-order) (TXL)
000B ¹⁶	Port P5 direction register (P5D)	002B ¹⁶	Timer X (high-order) (TXH)
000C ¹⁶	Port P6 (P6)	002C ¹⁶	Timer X (extension) (TXEX)
000D ¹⁶	Port P6 direction register (P6D)	002D ¹⁶	Timer Y (low-order) (TYL)
000E ¹⁶		002E ¹⁶	Timer Y (high-order) (TYH)
000F ¹⁶		002F ¹⁶	Timer X mode register (TXM)
0010 ¹⁶		0030 ¹⁶	Timer Y mode register (TYM)
0011 ¹⁶		0031 ¹⁶	
0012 ¹⁶		0032 ¹⁶	
0013 ¹⁶		0033 ¹⁶	
0014 ¹⁶		0034 ¹⁶	
0015 ¹⁶		0035 ¹⁶	
0016 ¹⁶		0036 ¹⁶	
0017 ¹⁶		0037 ¹⁶	Watchdog timer control register (WDTCON)
0018 ¹⁶	Clock output control register (CKOUT)	0038 ¹⁶	LCD power control register (VLCON)
0019 ¹⁶	A-D control register (ADCON)	0039 ¹⁶	LCD mode register (LM)
001A ¹⁶	A-D conversion register (low-order) (ADL)	003A ¹⁶	Interrupt edge selection register (INTEDGE)
001B ¹⁶	A-D conversion register (high-order) (ADH)	003B ¹⁶	CPU mode register (CPUM)
001C ¹⁶	Transmit/receive buffer register 1 (TB1/RB1)	003C ¹⁶	Interrupt request register 1 (IREQ1)
001D ¹⁶	Serial I/O1 status register (SIO1STS)	003D ¹⁶	Interrupt request register 2 (IREQ2)
001E ¹⁶	Transmit/receive buffer register 2 (TB2/RB2)	003E ¹⁶	Interrupt control register 1 (ICON1)
001F ¹⁶	Serial I/O2 status register (SIO2STS)	003F ¹⁶	Interrupt control register 2 (ICON2)
0FE0 ¹⁶	Serial I/O1 control register (SIO1CON)	0FF0 ¹⁶	Oscillation output control register (OSCOUT)
0FE1 ¹⁶	UART1 control register (UART1CON)	0FF1 ¹⁶	PULL register (PULL)
0FE2 ¹⁶	Baudrate generator 1 (BRG1)	0FF2 ¹⁶	Key input control register (KIC)
0FE3 ¹⁶	Serial I/O2 control register (SIO2CON)	0FF3 ¹⁶	Timer 1234 mode register (T1234M)
0FE4 ¹⁶	UART2 control register (UART2CON)	0FF4 ¹⁶	Timer X control register (TXCON)
0FE5 ¹⁶	Baudrate generator 2 (BRG2)	0FF5 ¹⁶	Timer 12 frequency division selection register (PRE12)
0FE6 ¹⁶		0FF6 ¹⁶	Timer 34 frequency division selection register (PRE34)
0FE7 ¹⁶		0FF7 ¹⁶	Timer XY frequency division selection register (PREXY)
0FE8 ¹⁶		0FF8 ¹⁶	Segment output disable register 0 (SEG0)
0FE9 ¹⁶		0FF9 ¹⁶	Segment output disable register 1 (SEG1)
0FEA ¹⁶		0FFA ¹⁶	Segment output disable register 2 (SEG2)
0FEB ¹⁶		0FFB ¹⁶	Timer Y mode register 2 (TYM2)
0FEC ¹⁶		0FFC ¹⁶	
0FED ¹⁶		0FFD ¹⁶	
0FEE ¹⁶		0FFE ¹⁶	Flash memory control register (FMCR)
0FEF ¹⁶		0FFF ¹⁶	Reserved area

Fig. 9 Memory map of special function register (SFR)

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I/O PORTS

Direction Registers

The I/O ports P0–P6 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When “0” is written to the bit of the direction register, the corresponding pin becomes an input pin. As for ports P0–P2, when “1” is written to the bit of the direction register and the segment output disable register, the corresponding pin becomes an output pin. As for ports P3–P6, when “1” is written to the bit of the direction register, the corresponding pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pull-up Control

Each individual bit of ports P0–P2 can be pulled up with a program by setting direction registers and segment output disable registers 0 to 2 (addresses 0FF816 to 0FFA16).

The pin is pulled up by setting “0” to the direction register and “1” to the segment output disable register.

By setting the PULL register (address 0FF116), ports P3–P6 can control pull-up with a program.

However, the contents of PULL register do not affect ports programmed as the output ports.

Segment output disable register Direction register	“0”	“1”	Initial state
“0”	Input port No pull-up	Input port Pull-up	
“1”	Segment output	Port output	

Fig. 10 Structure of ports P0 to P2

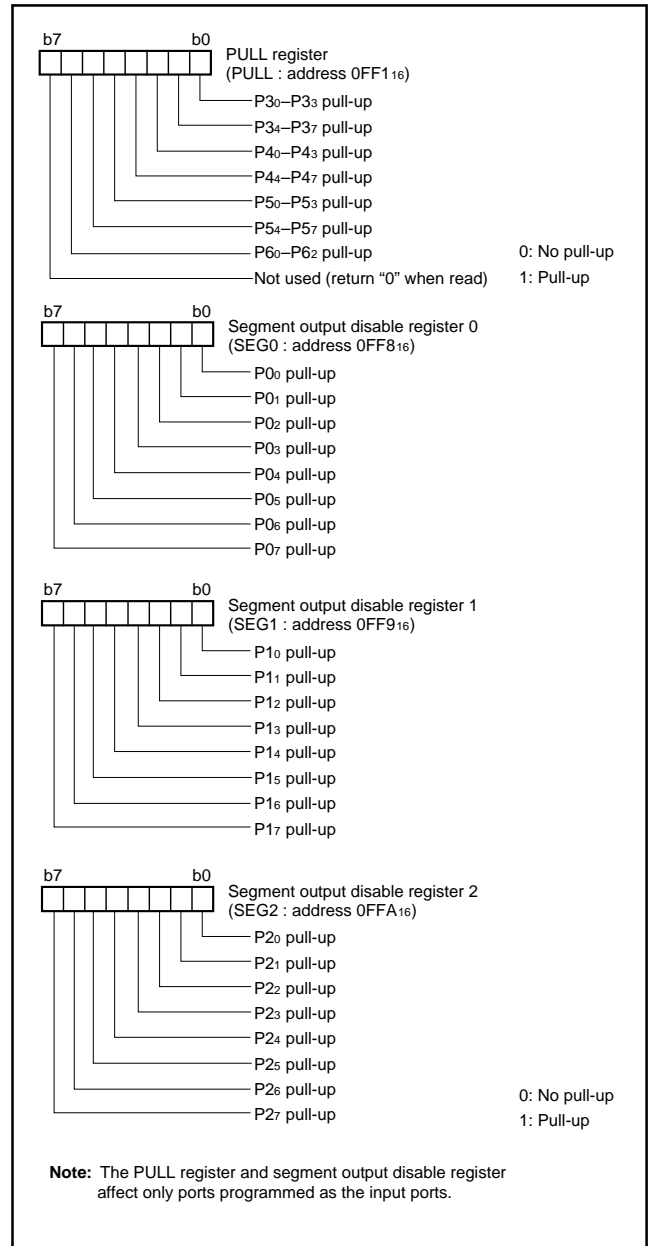


Fig. 11 Structure of PULL register and segment output disable register

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Table 6 List of I/O port function

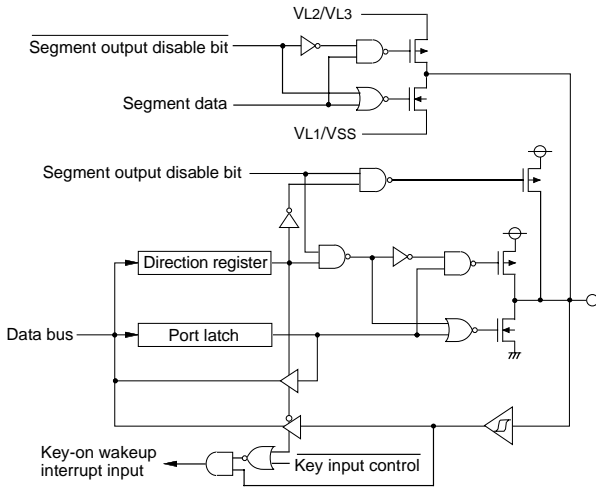
Pin	Name	Input/Output	I/O format	Non-port function		Related SFRs	Ref. No.	
P00/SEG0 – P03/SEG3	Port P0	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	LCD segment output	Key input (key-on wakeup) interrupt input	Segment output disable register 1	(1)	
							(2)	
P04/SEG4 – P07/SEG7								
P10/SEG8 – P17/SEG15	Port P1	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			Segment output disable register 2		
P20/SEG16 – P25/SEG21	Port P2	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output		LCD power input	Segment output disable register 3		
P26/SEG22/VL1								
P27/SEG23/VL2								
P30/SRDY2 P31/SCLK2 P32/TxD2 P33/RxD2	Port P3	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O		PULL register Serial I/O2 control register Serial I/O2 status register UART2 control register	(3) (4) (5) (6)	
P34/INT2				External interrupt input		PULL register Interrupt edge selection register	(7)	
P35/TXOUT P36/T2OUT/φ				Timer X output Timer 2 output		PULL register Timer X mode register Timer 12 mode register	(8) (9)	
P37/CNTR0				Timer X function input		PULL register Timer X mode register	(7)	
P40/OOUT0/AN0 P41/OOUT1/AN1	Port P4	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input	Oscillation external output	PULL register A-D control register	(11)	
P42/AN2– P45/AN5								(10)
P46/RTP0/AN6 P47/RTP1/AN7						Real time port function output	PULL register A-D control register Timer Y mode register	(11)
P50/INT0 P51/INT1	Port P5	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input		PULL register Interrupt edge selection register	(7)	
P52/T3OUT/PWM0 P53/T4OUT/PWM1				Timer 3 output Timer 4 output PWM output		PULL register Timer 12 mode register	(9)	
P54/RxD1 P55/TxD1 P56/SCLK1 P57/SRDY1				Serial I/O1 function I/O	Key input (key-on wakeup) interrupt input	PULL register Serial I/O1 control register Serial I/O1 status register UART1 control register	(12) (13) (14) (15)	
P60/CNTR1	Port P6	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Timer Y function input		PULL register Timer Y mode register	(7)	
P61/XCIN				Sub-clock oscillation circuit		PULL register	(16)	
P62/XCOUT						CPU mode register	(17)	
COM0–COM3	Common	Output	LCD common output			LCD mode register	(18)	

Notes 1: For details of how to use double/triple function ports as function I/O ports, refer to the applicable sections.

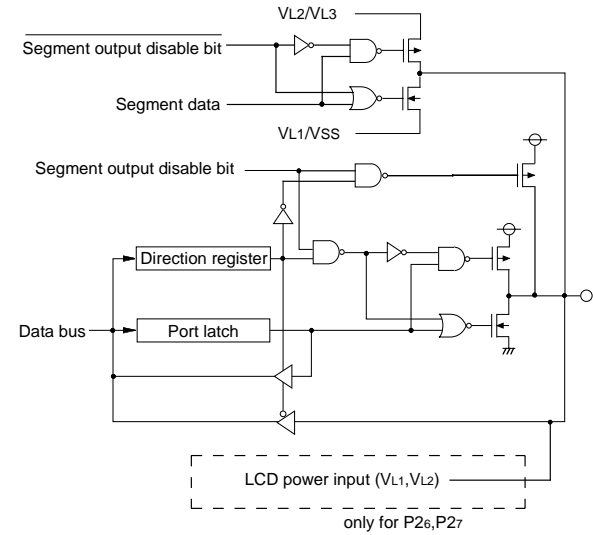
2: Make sure that the input level at each pin is either 0 V or VCC during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from VCC to VSS through the input-stage gate.

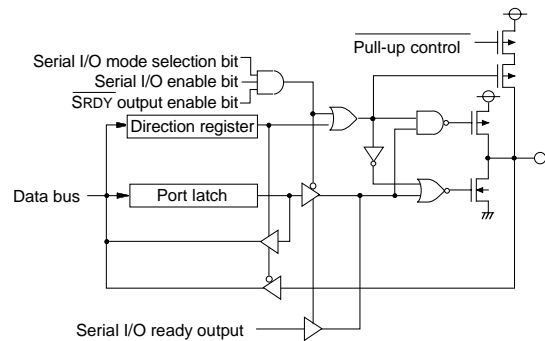
(1) Ports P00–P03



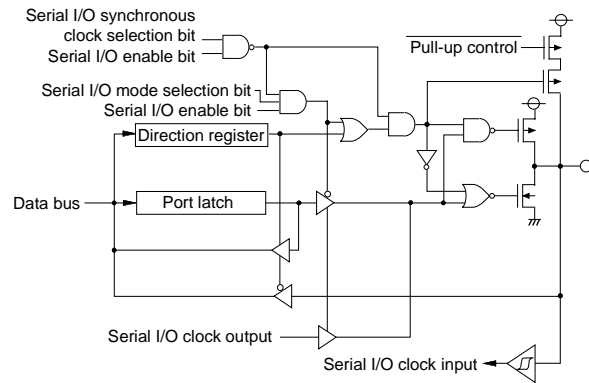
(2) Ports P04–P07, P1, P2



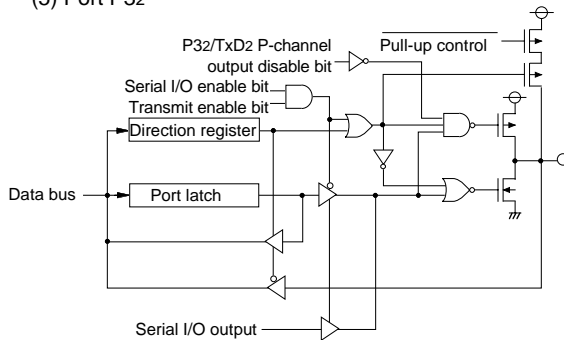
(3) Port P30



(4) Port P31



(5) Port P32



(6) Port P33

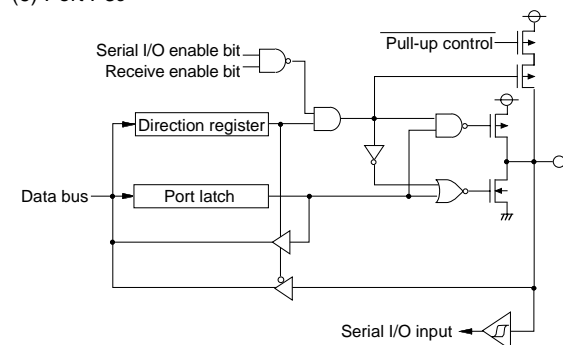


Fig. 12 Port block diagram (1)

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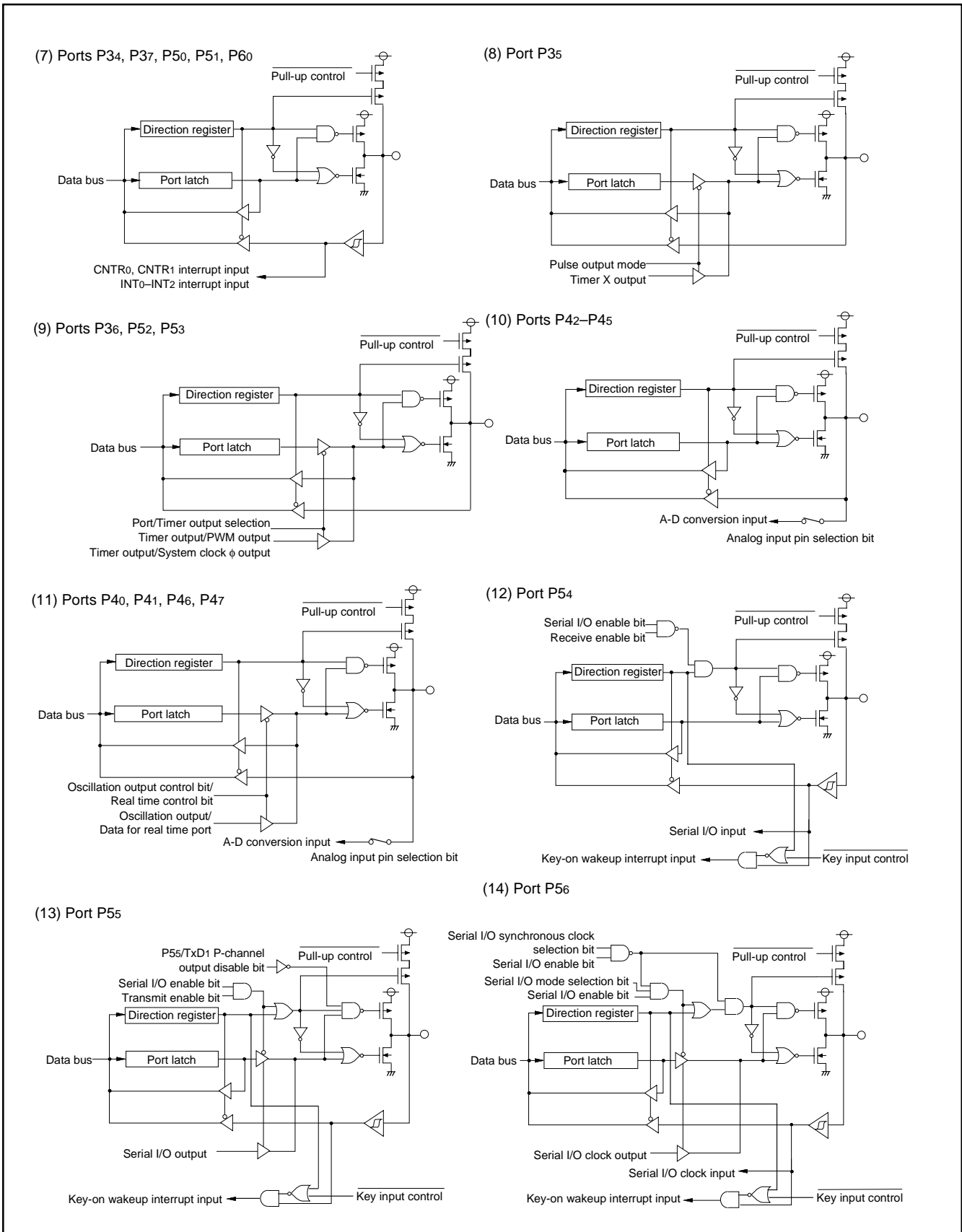


Fig. 13 Port block diagram (2)

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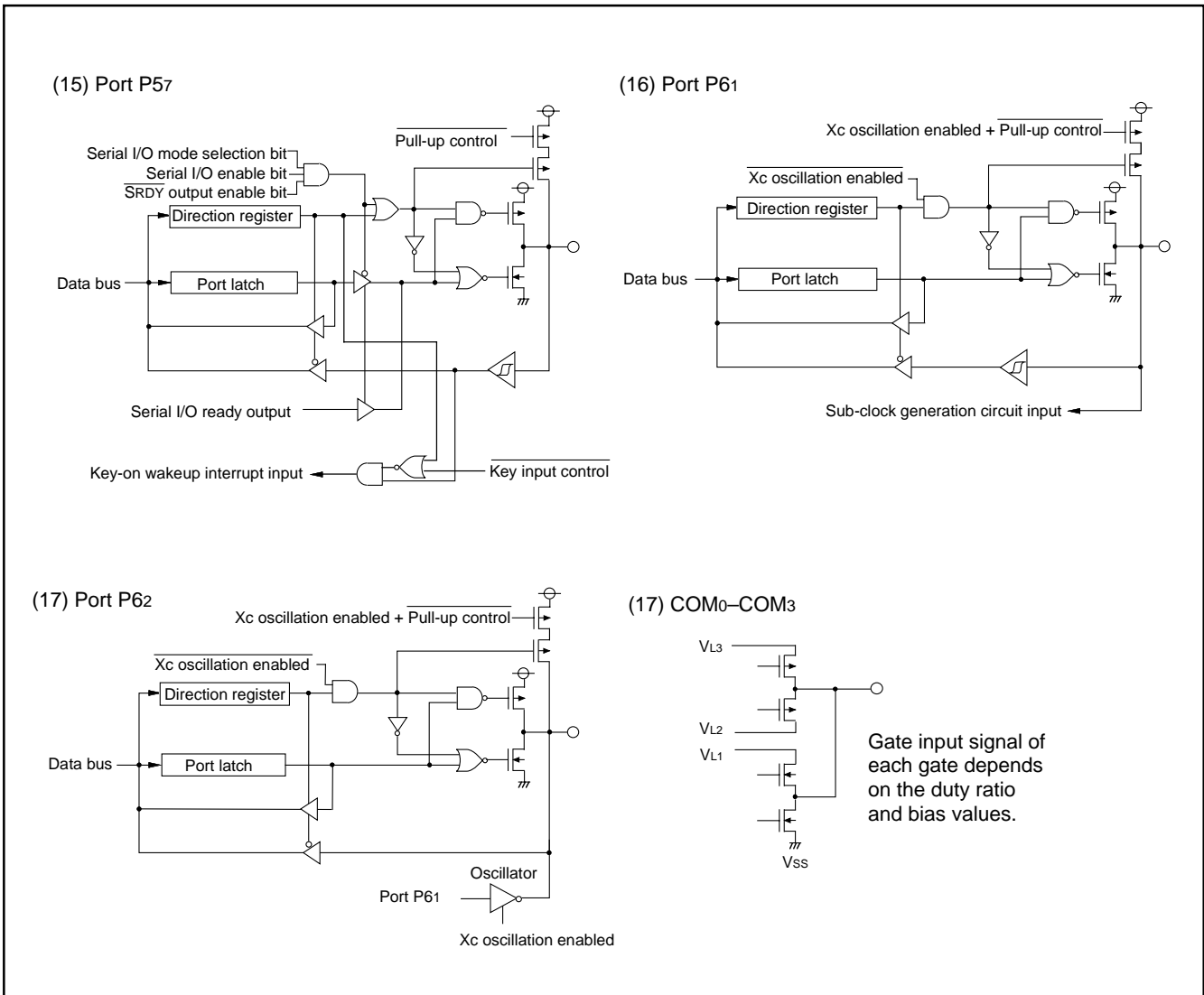


Fig. 14 Port block diagram (3)

PRELIMINARY
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 Some parametric limits are subject to change.

INTERRUPTS

Interrupts occur by nineteen sources: six external, twelve internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. The interrupt jump destination address is read from the vector table into the program counter.

Notes on Interrupts

When the active edge of an external interrupt (INT0 – INT2, CNTR0 or CNTR1) is set or an interrupt source where several interrupt source is assigned to the same vector address is switched, the corresponding interrupt request bit may also be set. Therefore, take following sequence:

- (1) Disable the interrupt.
- (2) Set the interrupt edge selection register (Timer X control register for CNTR0, Timer Y mode register for CNTR1).
- (3) Clear the set interrupt request bit to "0."
- (4) Enable the interrupt.

Table 7 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT0	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
INT2	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT2 input	Valid when INT2 interrupt is selected External interrupt (active edge selectable)
Key input (key-on wakeup)				At falling of ports P00–P03, P54–P57 input logical level AND	Valid when key input interrupt is selected External interrupt (falling valid)
Serial I/O1 receive	5	FFF5 ₁₆	FFF4 ₁₆	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	6	FFF3 ₁₆	FFF2 ₁₆	At completion of serial I/O1 transmit shift or transmit buffer is empty	Valid only when serial I/O1 is selected
Serial I/O2 receive	7	FFF1 ₁₆	FFF0 ₁₆	At completion of serial I/O2 data receive	Valid only when serial I/O2 is selected
Serial I/O2 transmit	8	FFEF ₁₆	FFEE ₁₆	At completion of serial I/O2 transmit shift or transmit buffer is empty	Valid only when serial I/O2 is selected
Timer X	9	FFED ₁₆	FFEC ₁₆	At timer X underflow	
Timer 1	10	FFEB ₁₆	FFEA ₁₆	At timer 1 underflow	Valid only when timer 1 interrupt is selected
Timer 2	11	FFE9 ₁₆	FFE8 ₁₆	At timer 2 underflow	Valid only when timer 2 interrupt is selected
Timer 3	12	FFE7 ₁₆	FFE6 ₁₆	At timer 3 underflow	
Timer 4	13	FFE5 ₁₆	FFE4 ₁₆	At timer 4 underflow	
CNTR0	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
Timer Y CNTR1	15	FFE1 ₁₆	FFE0 ₁₆	At timer Y underflow At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
A-D conversion	16	FFDF ₁₆	FFDE ₁₆	At completion of A-D conversion	Valid when A-D conversion interrupt is selected
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

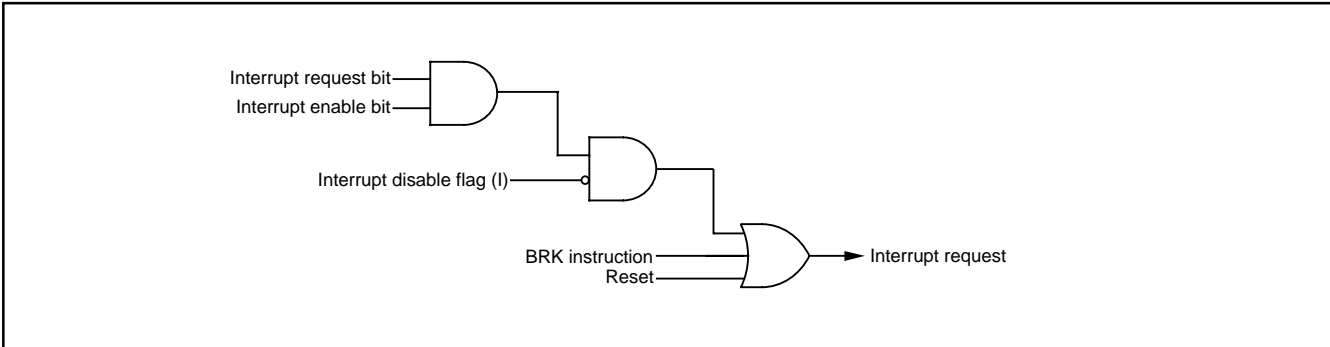


Fig. 15 Interrupt control

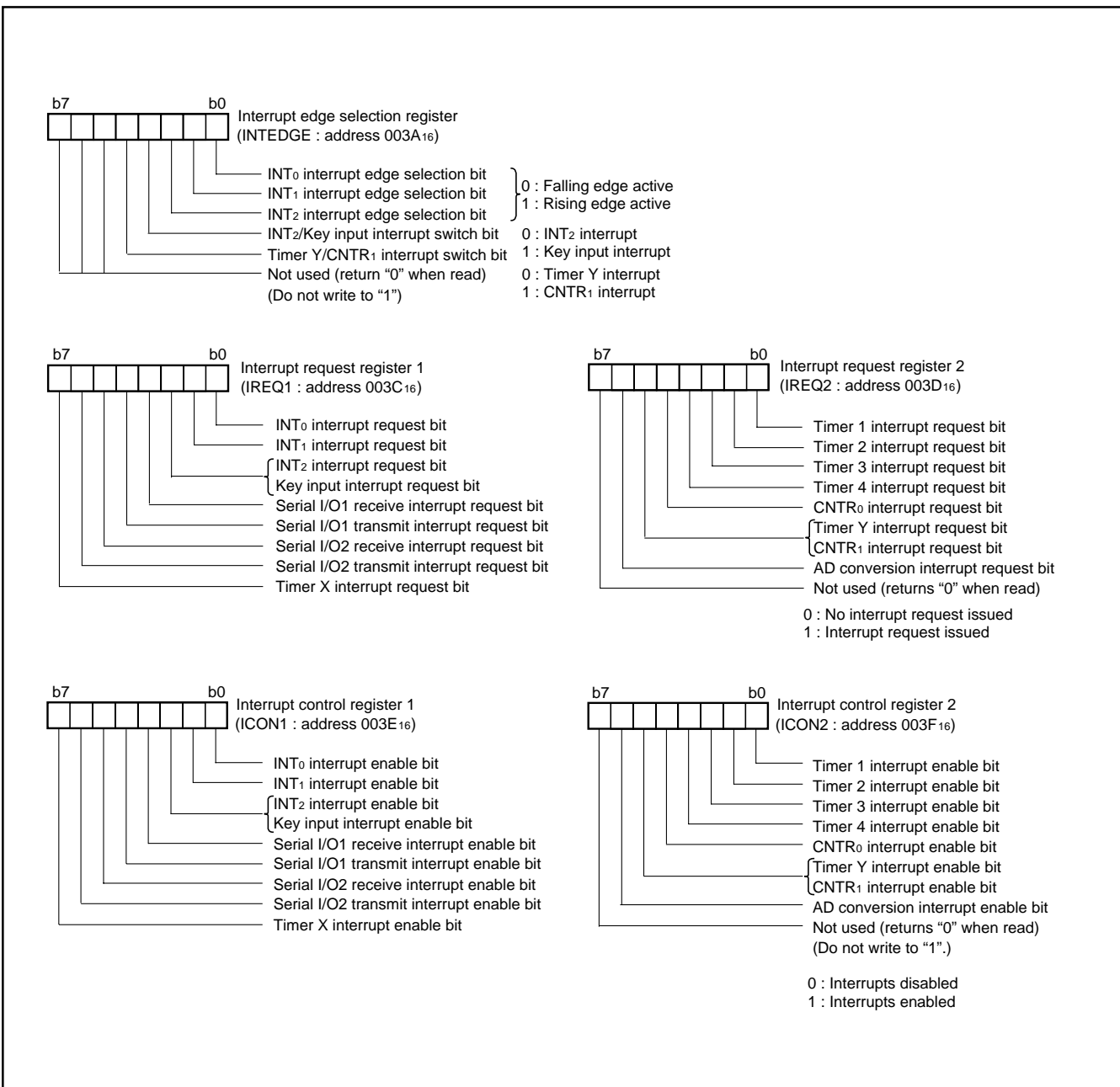


Fig. 16 Structure of interrupt-related registers

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by detecting the falling edge from any pin of ports P00–P03, P54–P57 that have been set to input mode. In other words, it is generated when AND of input level

goes from "1" to "0". An example of using a key input interrupt is shown in Figure 17, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P54–P57.

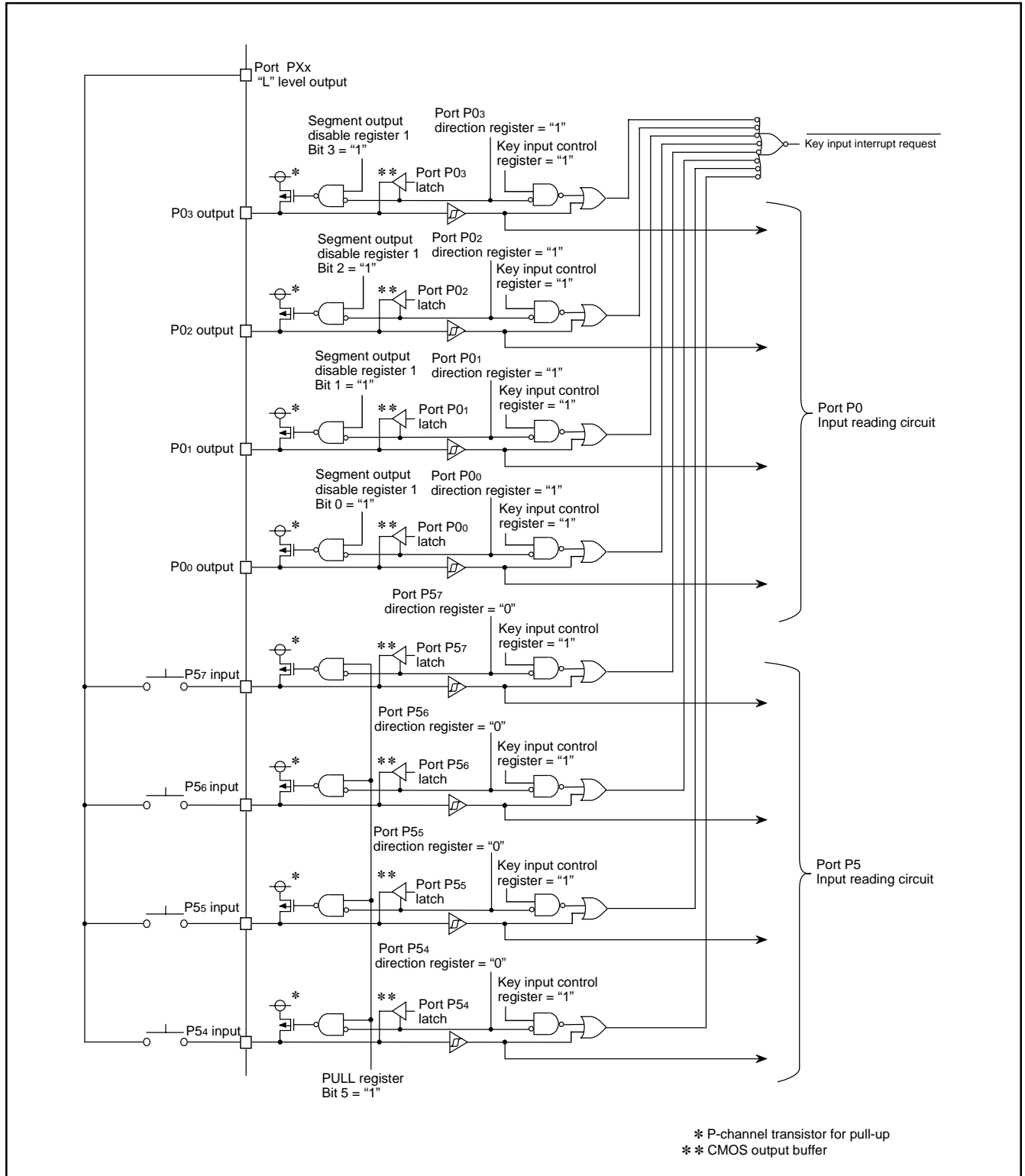


Fig. 17 Connection example when using key input interrupt and ports P0 and P5 block diagram

A key input interrupt is controlled by the key input control register and port direction registers. When the key input interrupt is enabled, set "1" to the key input control register. A key input of any pin of ports P0₀–P0₃, P5₄–P5₇ that have been set to input mode is accepted.

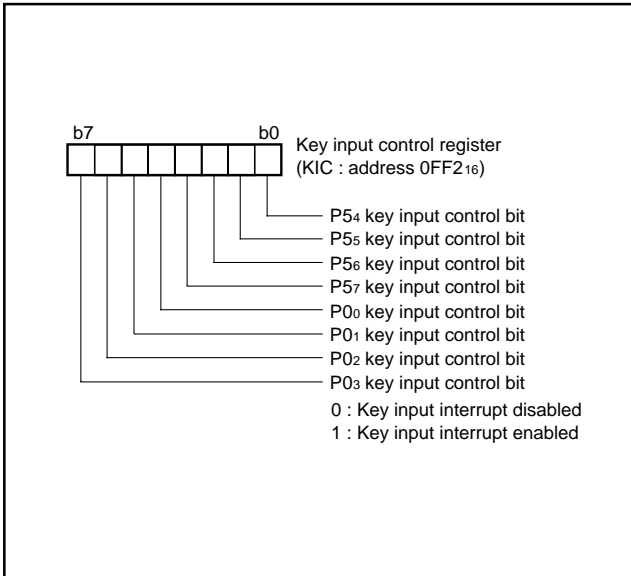


Fig. 18 Structure of key input control register

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TIMERS

8-Bit Timer

The 38C2 group has four built-in timers : Timer 1, Timer 2, Timer 3, and Timer 4.

Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches "00₁₆," the contents of the timer latch is reloaded into the timer with the next count pulse. In this mode, the interrupt request bit corresponding to that timer is set to "1."

The count can be stopped by setting the stop bit of each timer to "1."

● Frequency Divider For Timer

Timer 1, timer 2, timer 3 and timer 4 have the frequency divider for the count source. The count source of the frequency divider is switched to X_{IN} or X_{CIN} by the CPU mode register. The frequency divider is controlled by the 3-bit register. The division ratio can be selected from as follows;

1/1, 1/2, 1/16, 1/32, 1/64, 1/128, 1/256, 1/1024 of f(X_{IN}) or f(X_{CIN}).

●Timer 1, Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

When f(X_{CIN}) is selected as the count source, counting can be performed regardless of X_{CIN} oscillation. However, when X_{CIN} is stopped, the external pulse input from X_{CIN} pin is counted. Also, by the timer 12 mode register, each time timer 2 underflows, the signal of which polarity is inverted can be output from P₃₆/T_{2OUT} pin.

At reset, all bits of the timer 12 mode register are cleared to "0," timer 1 is set to "FF₁₆," and timer 2 is set to "01₁₆."

When executing the STP instruction, previously set the wait time at return.

● Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. Also, by the timer 34 mode register, each time timer 3 or timer 4 underflows, the signal of which polarity is inverted can be output from P₅₂/T_{3OUT} pin or P₅₃/T_{4OUT} pin.

● Timer 3 PWM₀ Mode, Timer 4 PWM₁ Mode

A PWM rectangular waveform corresponding to the 10-bit accuracy can be output from the P₅₂/PWM₀ pin and P₅₃/PWM₁ pin by setting the timer 34 mode register and PWM₀₁ register (refer to Figure 21).

The "n" is the value set in the timer 3 (address 0022₁₆) or the timer 4 (address 0023₁₆). The "ts" is one period of timer 3 or timer 4 count source.

One output pulse is the short interval. Four output pulses are the long interval. "H" width of the short interval is obtained by n X ts.

However, in the long interval, "H" width of output pulse is extended for ts which is set by the PWM₀₁ register (address 0024₁₆).

PRELIMINARY
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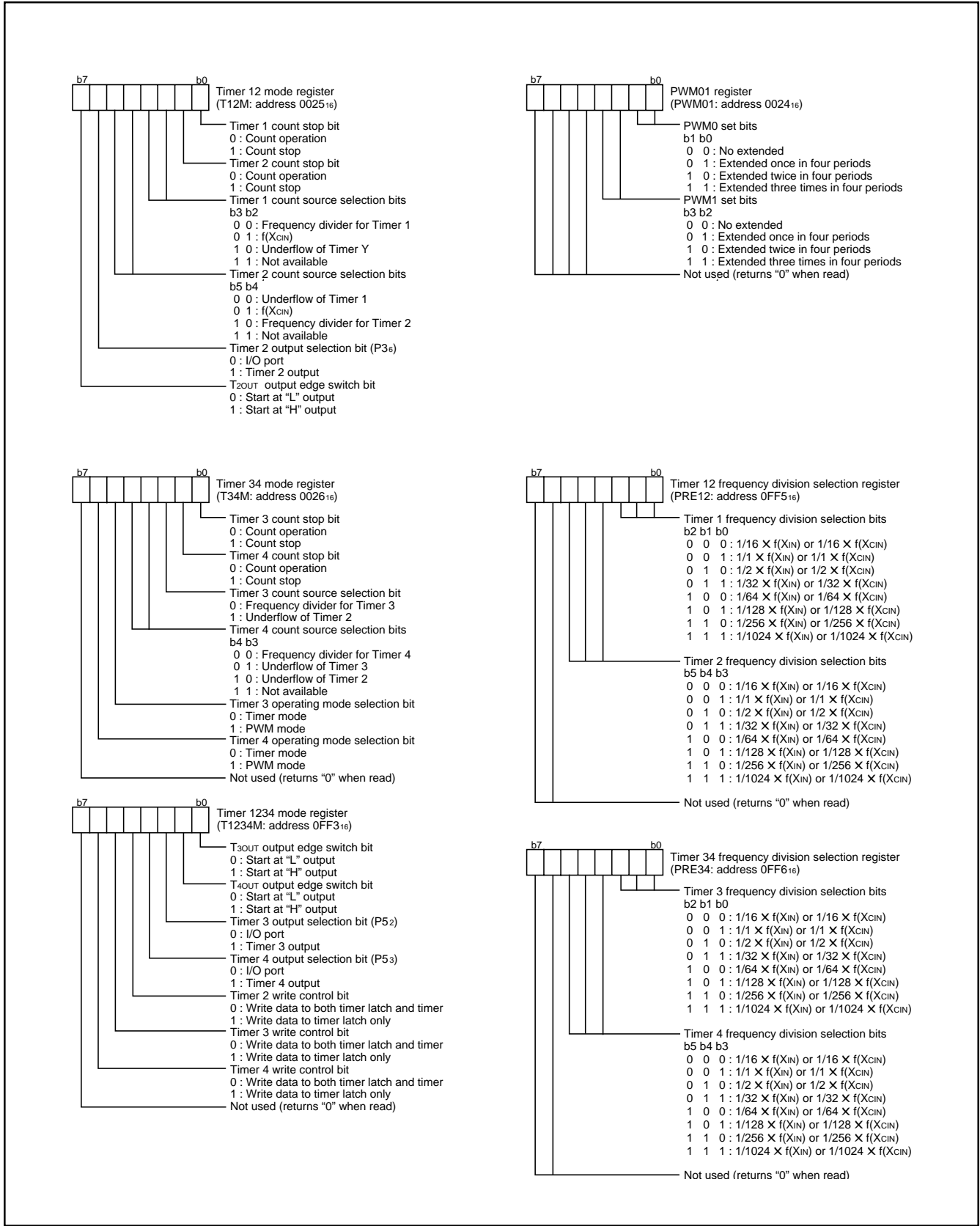


Fig. 19 Structure of timer related register

PRELIMINARY
 Notice: This is not a final specification.
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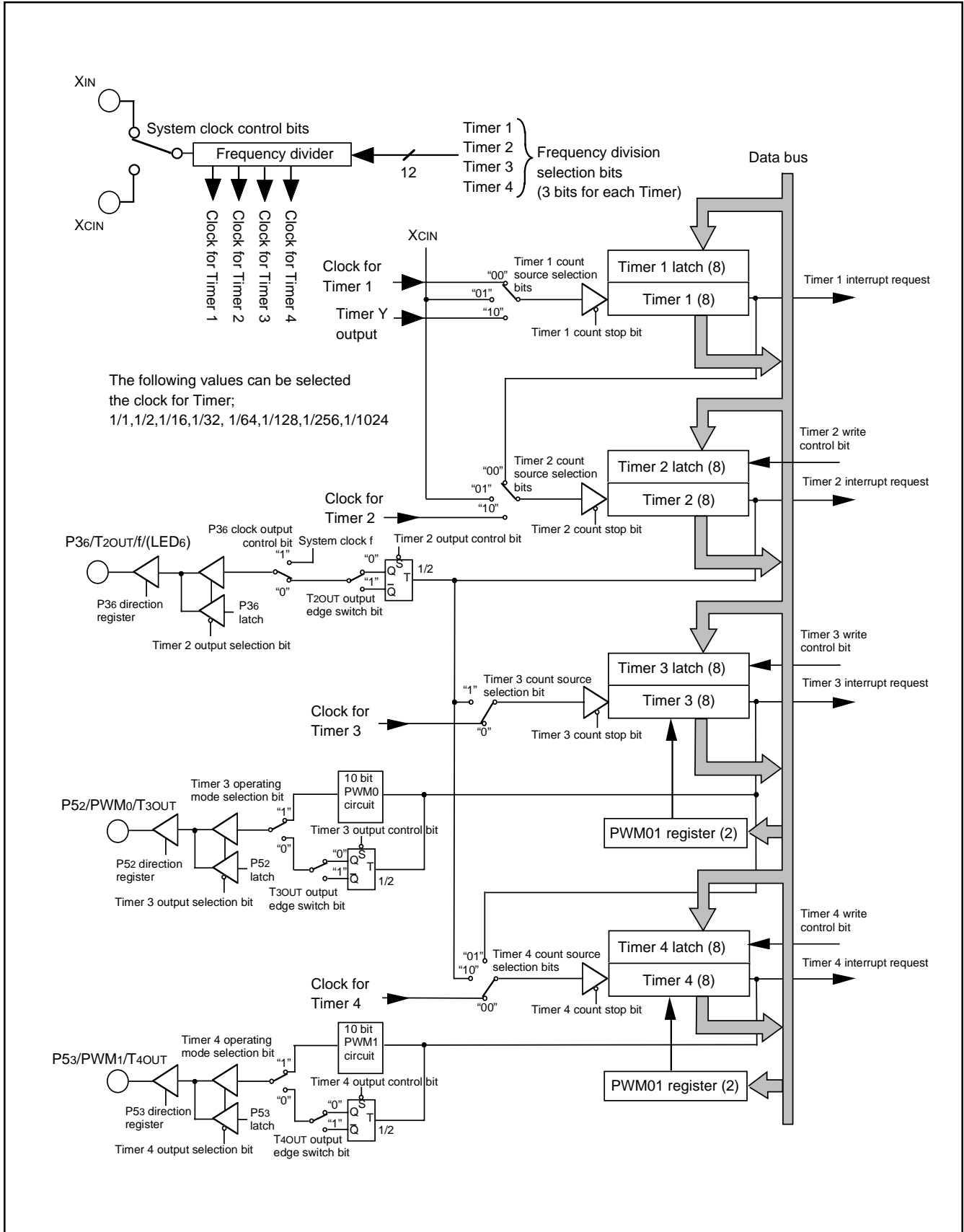


Fig. 20 Block diagram of timers 1, 2, 3 and 4

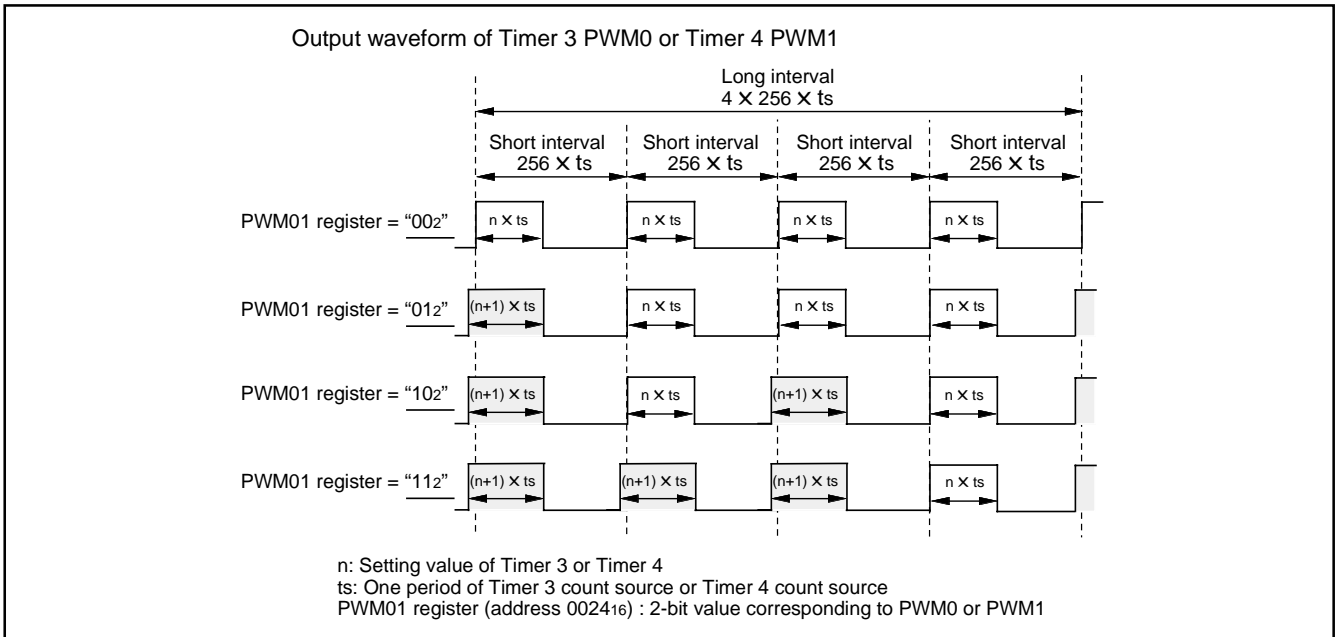


Fig. 21 Waveform of PWM01

16-bit Timer

● **Frequency Divider For Timer**

Each timer X and timer Y have the frequency dividers for the count source. The count source of the frequency divider is switched to XIN or XCIN by the CPU mode register. The division ratio of each timer can be controlled by the 3-bit register. The division ratio can be selected from as follows;

1/1, 1/2, 1/16, 1/32, 1/64, 1/128, 1/256, 1/1024 of $f(XIN)$ or $f(XCIN)$.

● **Timer X**

The timer X count source can be selected by setting the timer X mode register. When $f(XCIN)$ is selected as the count source, counting can be performed regardless of XCIN oscillation. However, when XCIN is stopped, the external pulse input from XCIN pin is counted.

The timer X operates as down-count. When the timer contents reach "0000₁₆", an underflow occurs at the next count pulse and the timer latch contents are reloaded. After that, the timer continues count-down. When the timer underflows, the interrupt request bit corresponding to the timer X is set to "1".

Six operating modes can be selected for timer X by the timer X mode register and timer X control register.

(1) Timer Mode

The count source can be selected by setting the timer X mode register. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension).

(2) Pulse Output Mode

Pulses of which polarity is inverted each time the timer underflows are output from the TXOUT pin. Except for that, this mode operates just as in the timer mode.

When using this mode, set the port sharing the TXOUT pin to output mode.

(3) IGBT Output Mode

After dummy output from the TXOUT pin, count starts with the INT0 pin input as a trigger. In the case that the timer X output edge switch bit is "0", when the trigger is detected or the timer X underflows, "H" is output from the TXOUT pin. When the count value corresponds with the compare register value, the TXOUT output becomes "L".

After noise is cleared by noise filters, judging continuous 4-time same levels with sampling clocks to be signals, the INT0 signal can use 4 types of delay time by a delay circuit.

When using this mode, set the port sharing the INT0 pin to input mode and set the port sharing the TXOUT pin to output mode.

When the timer X output control bit 1 or 2 of the timer X control register is set to "1", the timer X count stop bit is fixed to "1" forcibly by the interrupt signal of INT1 or INT2. And then, by stopping the timer X counting, the TXOUT output can be fixed to the signal output at that time.

Do not write "1" to the timer X register (extension) when using the IGBT output mode.

(4) PWM Mode

IGBT dummy output, an external trigger with the INT0 pin and output control with pins INT1 and INT2 are not used. Except for those, this mode operates just as in the IGBT output mode.

The period of PWM waveform is specified by the timer X set value. In the case that the timer X output edge switch bit is "0", the "H" interval is specified by the compare register set value.

When using this mode, set the port sharing the TXOUT pin to output mode.

Do not write "1" to the timer X register (extension) when using the PWM mode.

PRELIMINARY
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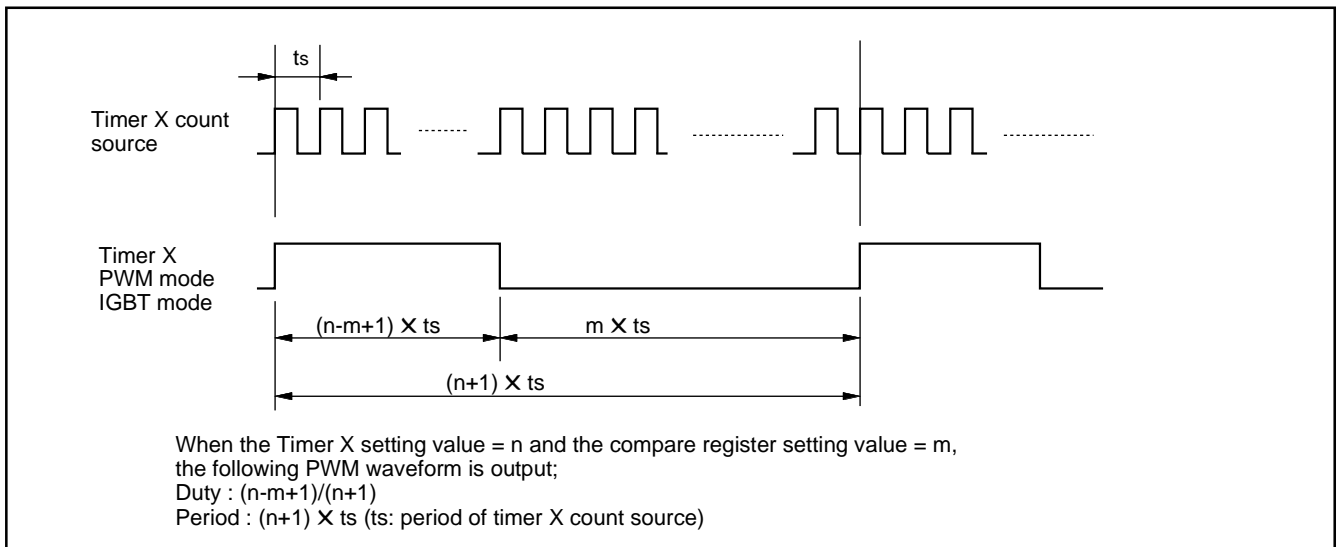


Fig. 22 Waveform of PWM/IGBT

(5) Event Counter Mode

The timer counts signals input through the CNTR0 pin. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When using this mode, set the port sharing the CNTR0 pin to input mode.

In this mode, the window control can be performed by the timer 1 underflow. When the bit 5 (data for control of event counter window) of the timer X mode register is set to "1", counting is stopped at the next timer 1 underflow. When the bit is set to "0", counting is re-started at the next timer 1 underflow.

(6) Pulse Width Measurement Mode

In this mode, the count source is the output of frequency divider for timer. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When the bit 6 of the CNTR0 active edge switch bits is "0", counting is executed during the "H" interval of CNTR0 pin input. When the bit is "1", counting is executed during the "L" interval of CNTR0 pin input. When using this mode, set the port sharing the CNTR0 pin to input mode.

■ Notes on Timer X

(1) Write Order to Timer X

- In the timer mode, pulse output mode, event counter mode and pulse width measurement mode, write to the following registers in the order as shown below;
 the timer X register (extension),
 the timer X register (low-order),
 the timer X register (high-order).

Do not write to only one of them.

When the above mode is set and timer X operates as the 16-bit counter, if the timer X register (extension) is never set after reset is released, setting the timer X register (extension) is not required. In this case, write the timer X register (low-order) first and the timer X register (high-order). However, once writing to the timer X register is executed, note that the value is retained to the reload latch.

- In the IGBT and PWM modes, do not write "1" to the timer X register (extension). Also, when "1" is already written to the timer X register, be sure to write "0" to the register before using. Write to the following registers in the order as shown below;
 the compare register (high- and low-order),
 the timer X register (extension),
 the timer X register (low-order),
 the timer X register (high-order).
- It is possible to use whichever order to write to the compare register (high- and low-order). However, write both the compare register and the timer X register at the same time.

(2) Read Order to Timer X

- In all modes, read the following registers in the order as shown below;
 the timer X register (extension),
 the timer X register (high-order),
 the timer X register (low-order).
- When reading the timer X register (extension) is not required, read the timer X register (high-order) first and the timer X register (low-order).
- Read order to the compare register is not specified.
- If reading to the timer X register during write operation or writing to it during read operation is performed, normal operation will not be performed.

(3) Write to Timer X

- When writing a value to the timer X address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. Normally, when writing a value to the timer X address, the value is set into the timer and the timer latch at the same time, because they are written at the same time. When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

PRELIMINARY
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(4) Set of Timer X Mode Register

Set the write control bit of the timer X mode register to "1" (write to the latch only) when setting the IGBT output and PWM modes. Output waveform simultaneously reflects the contents of both registers at the next underflow after writing to the timer X register (high-order).

(5) Output Control Function of Timer X

When using the output control function (INT₁ and INT₂) in the IGBT output mode, set the levels of INT₁ and INT₂ to "H" in the falling edge active or to "L" in the rising edge active before switching to the IGBT output mode.

(6) Note on Switch of CNTR₀ Active Edge

- When the CNTR₀ active edge switch bits are set, at the same time, the interrupt active edge is also affected.
- When the pulse width is measured, set the bit 7 of the CNTR₀ active edge switch bits to "0".

Timer Y

Timer Y is a 16-bit timer.

The timer Y count source can be selected by setting the timer Y mode register. When f(XCIN) is selected as the count source, counting can be performed regardless of XCIN oscillation. However, when XCIN is stopped, the external pulse input from XCIN pin is counted.

Four operating modes can be selected for timer Y by the timer Y mode register. Also, the real time port can be controlled.

(1) Timer Mode

The timer Y count source can be selected by setting the timer Y mode register.

(2) Period Measurement Mode

The interrupt request is generated at rising/falling edge of CNTR₁ pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting. Except for that, this mode operates just as in the timer mode.

The timer value just before the reloading at rising/falling of CNTR₁ pin input is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR₁ pin input is found by CNTR₁ interrupt. When using this mode, set the port sharing the CNTR₁ pin to input mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR₁ pin.

Except for that, this mode operates just as in the timer mode.

When using this mode, set the port sharing the CNTR₁ pin to input mode.

(4) Pulse Width HL Continuously Measurement Mode

The interrupt request is generated at both rising and falling edges of CNTR₁ pin input signal. Except for that, this mode operates just as in the period measurement mode. When using this mode, set the port sharing the CNTR₁ pin to input mode.

■ Notes on Timer Y

● CNTR₁ Interrupt Active Edge Selection

CNTR₁ interrupt active edge depends on the CNTR₁ active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR₁ interrupt request is generated at both rising and falling edges of CNTR₁ pin input signal regardless of the setting of CNTR₁ active edge switch bit.

● Timer Y Read/Write Control

- When reading from/writing to timer Y, read from/write to both the high-order and low-order bytes of timer Y. When the value is read, read the high-order bytes first and the low-order bytes next. When the value is written, write the low-order bytes first and the high-order bytes next.

If reading from the timer Y register during write operation or writing to it during read operation is performed, normal operation will not be performed.

- When writing a value to the timer Y address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. Normally, when writing a value to the timer Y address, the value is set into the timer and the timer latch at the same time, because they are set to write at the same time.

When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.

- Do not switch the timer count source during timer count operation. Stop the timer count before switching it.

● Real Time Port Control

When the real time port function is valid, data for the real time port is output from ports P4₇ and P4₆ each time the timer Y underflows. (However, if the real time port control bit is changed from "0" to "1" after the data for real time port is set, data is output independent of the timer Y operation.) When the data for the real time port is changed while the real time port function is valid, the changed data is output at the next underflow of timer Y. Before using this function, set the corresponding port direction registers to output mode.

PRELIMINARY
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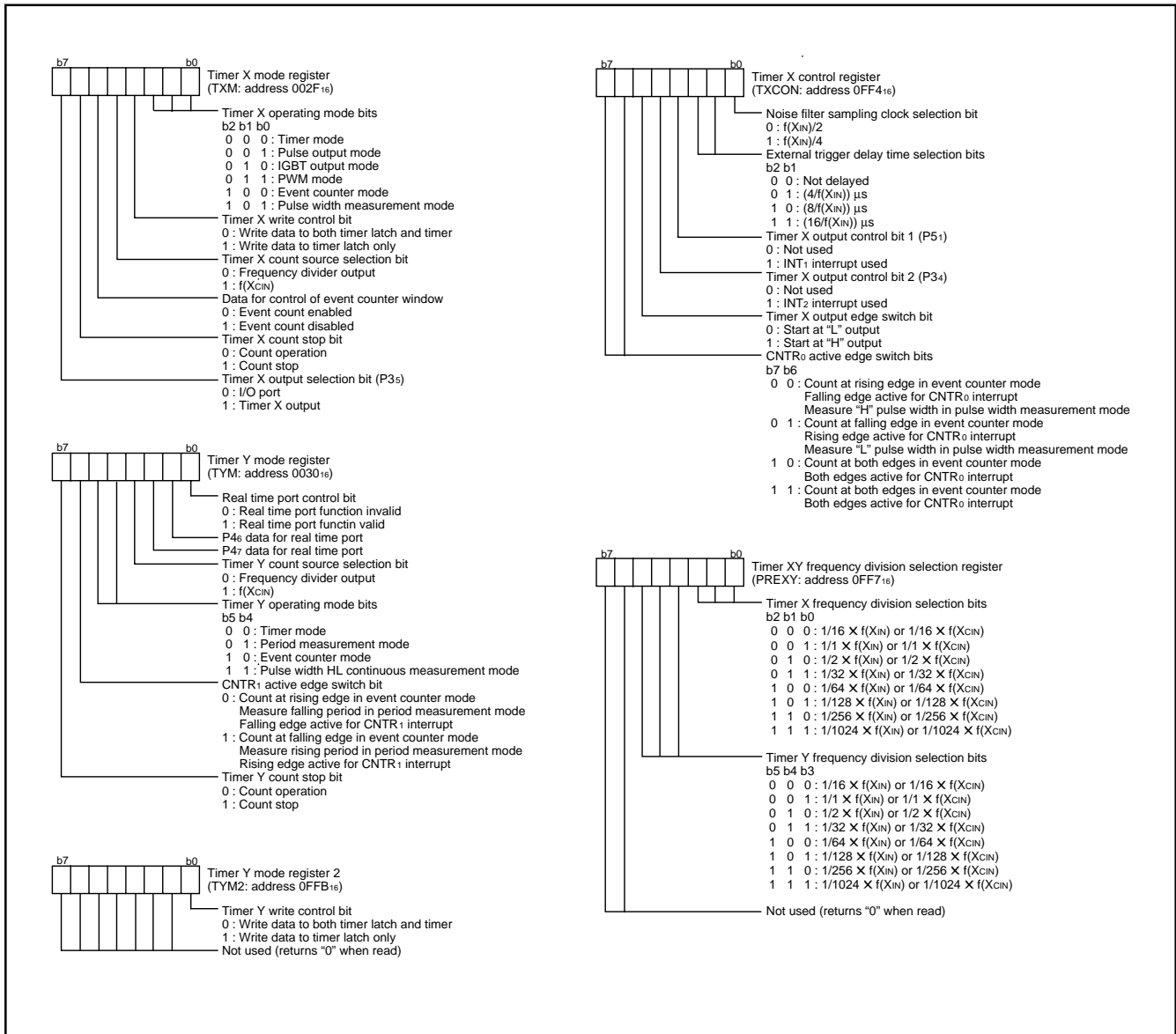


Fig. 23 Structure of Timer X, Y related registers

PRELIMINARY
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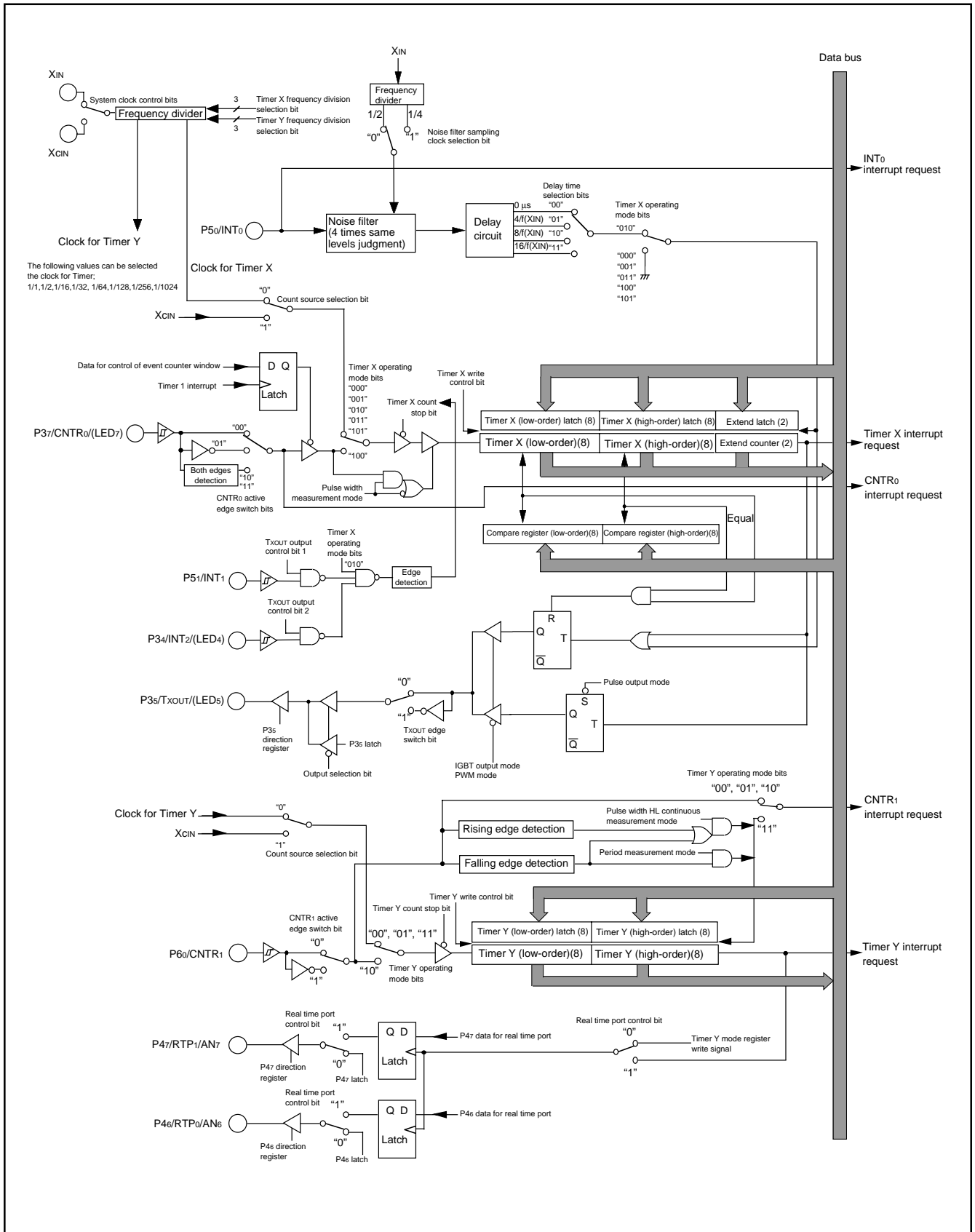


Fig. 24 Block diagram of Timer X, Y

SERIAL I/O

The 38C2 group has built-in two 8-bit serial I/O. Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register to "1". For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

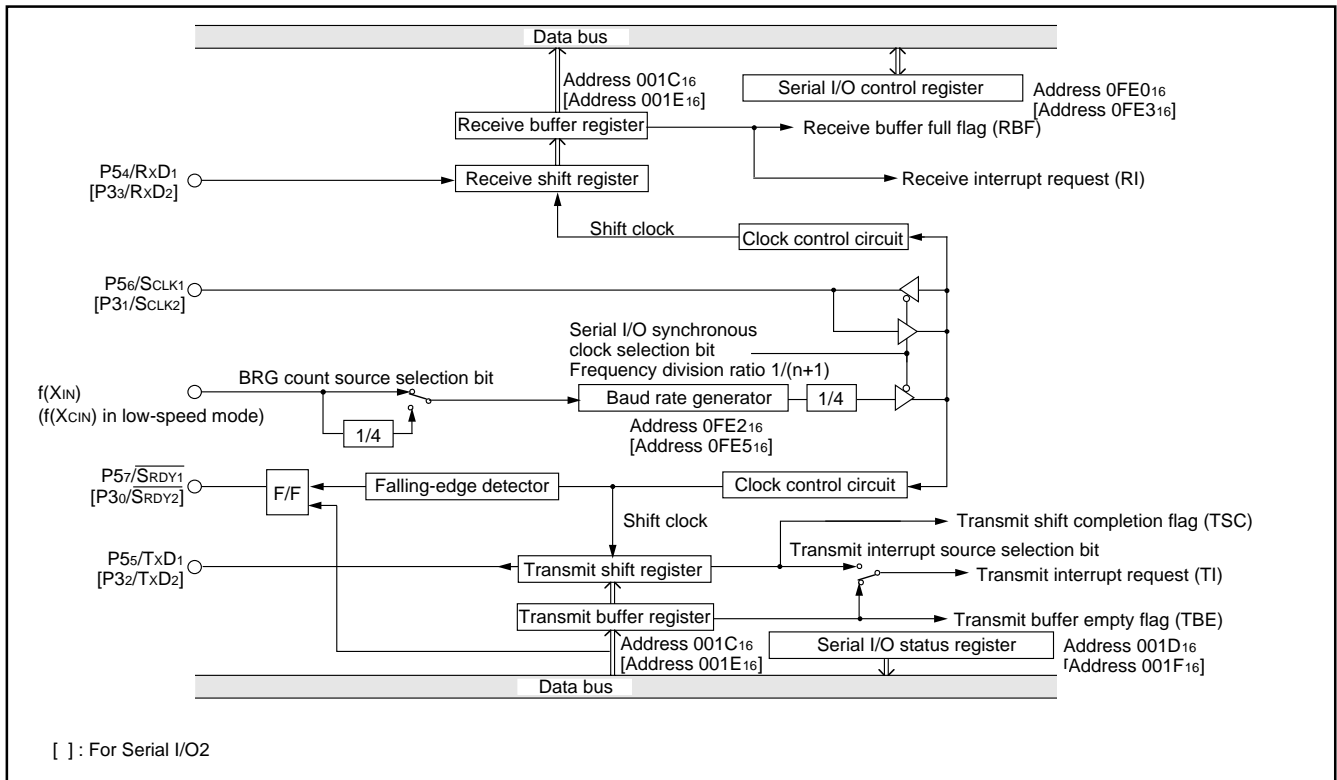


Fig. 25 Block diagram of clock synchronous serial I/O

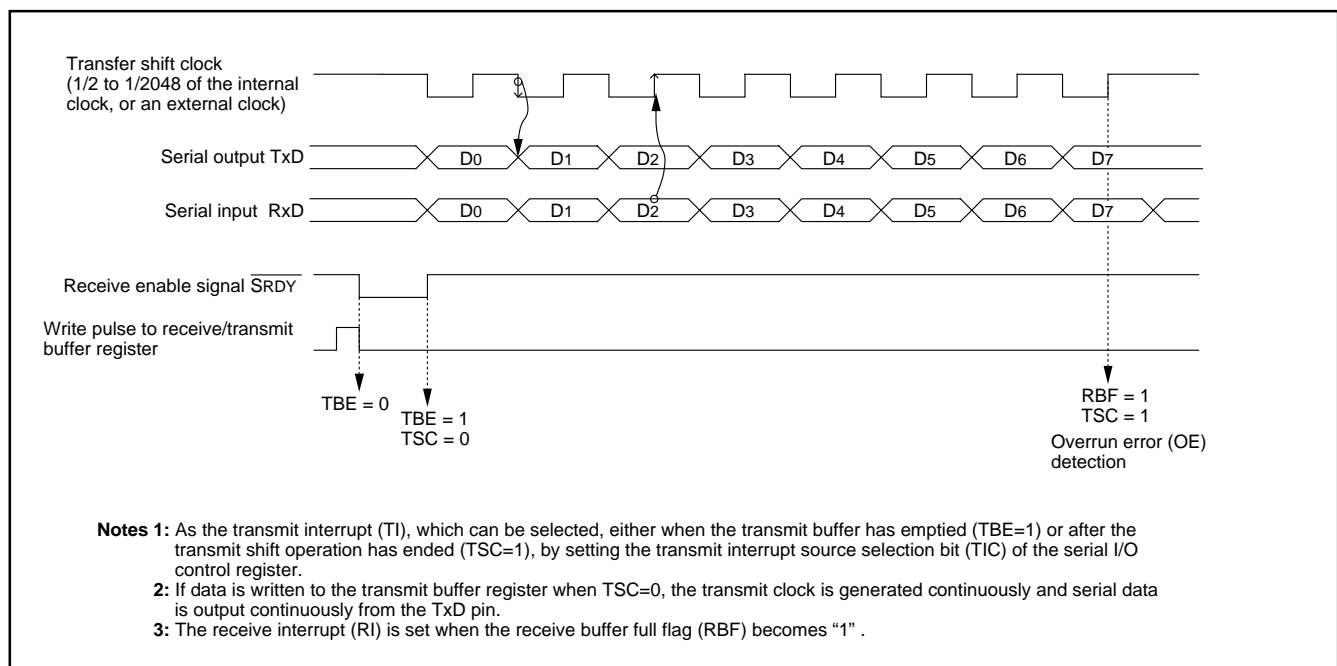


Fig. 26 Operation of clock synchronous serial I/O function

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

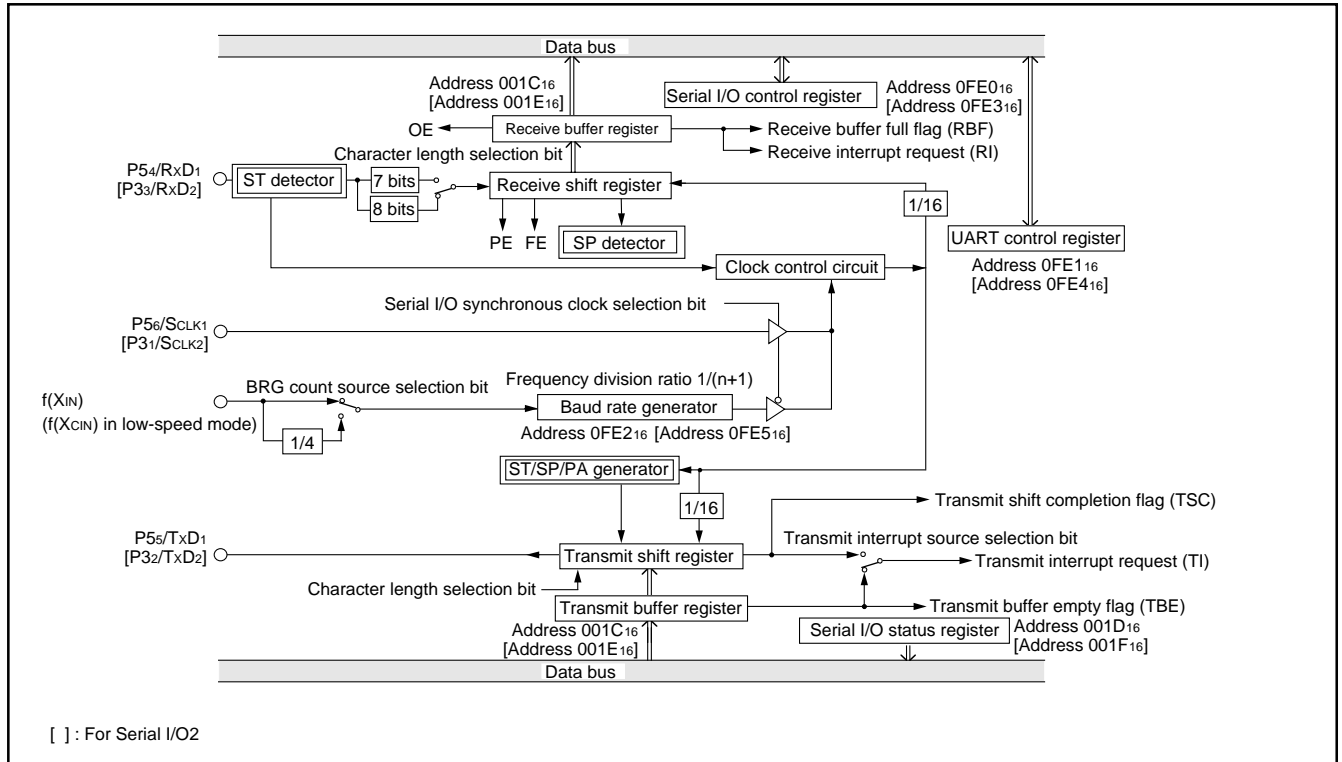
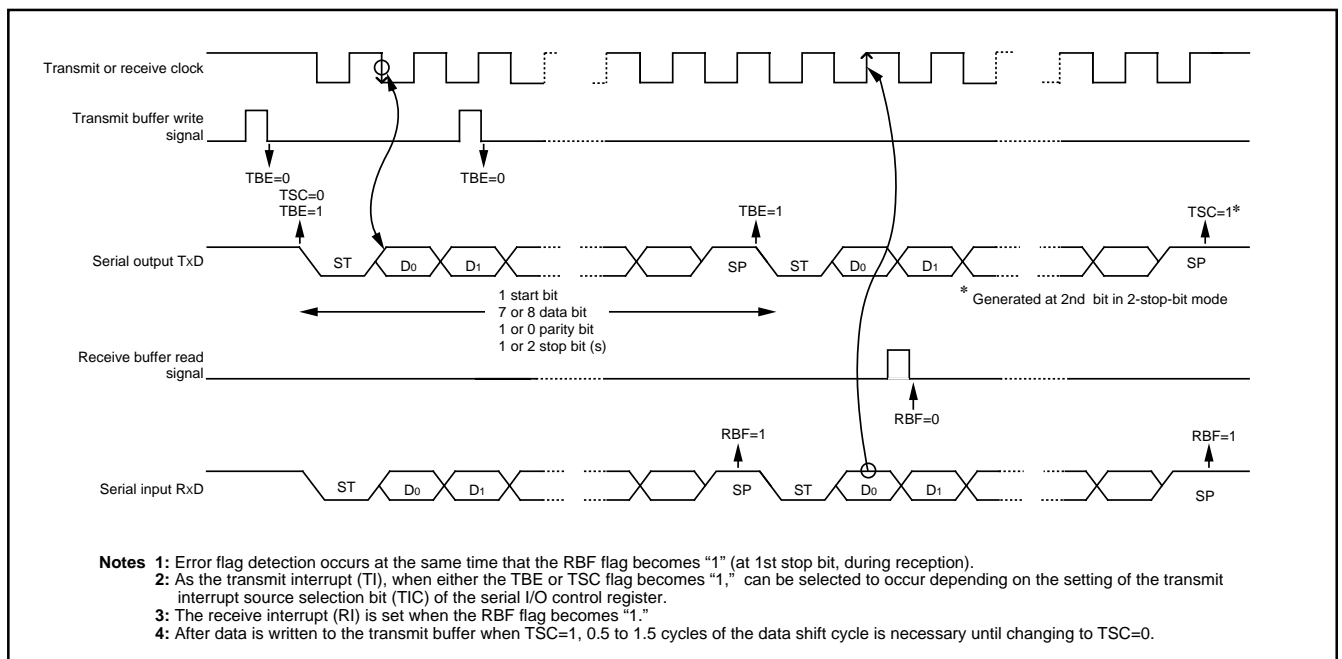


Fig. 27 Block diagram of UART serial I/O



- Notes**
- 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
 - 2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1," can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
 - 3: The receive interrupt (RI) is set when the RBF flag becomes "1."
 - 4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 28 Operation of UART serial I/O function

PRELIMINARY
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[Transmit Buffer Register/Receive Buffer Register (TB/RB)]

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O Status Register (SIO1STS, SIO2STS)]

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O Control Register (SIO1CON, SIO2CON)]

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART Control Register (UART1CON, UART2CON)]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P55/TxD1 [P32/TxD2] pin.

[Baud Rate Generator (BRG1, BRG2)]

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

PRELIMINARY
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 Some parametric limits are subject to change.

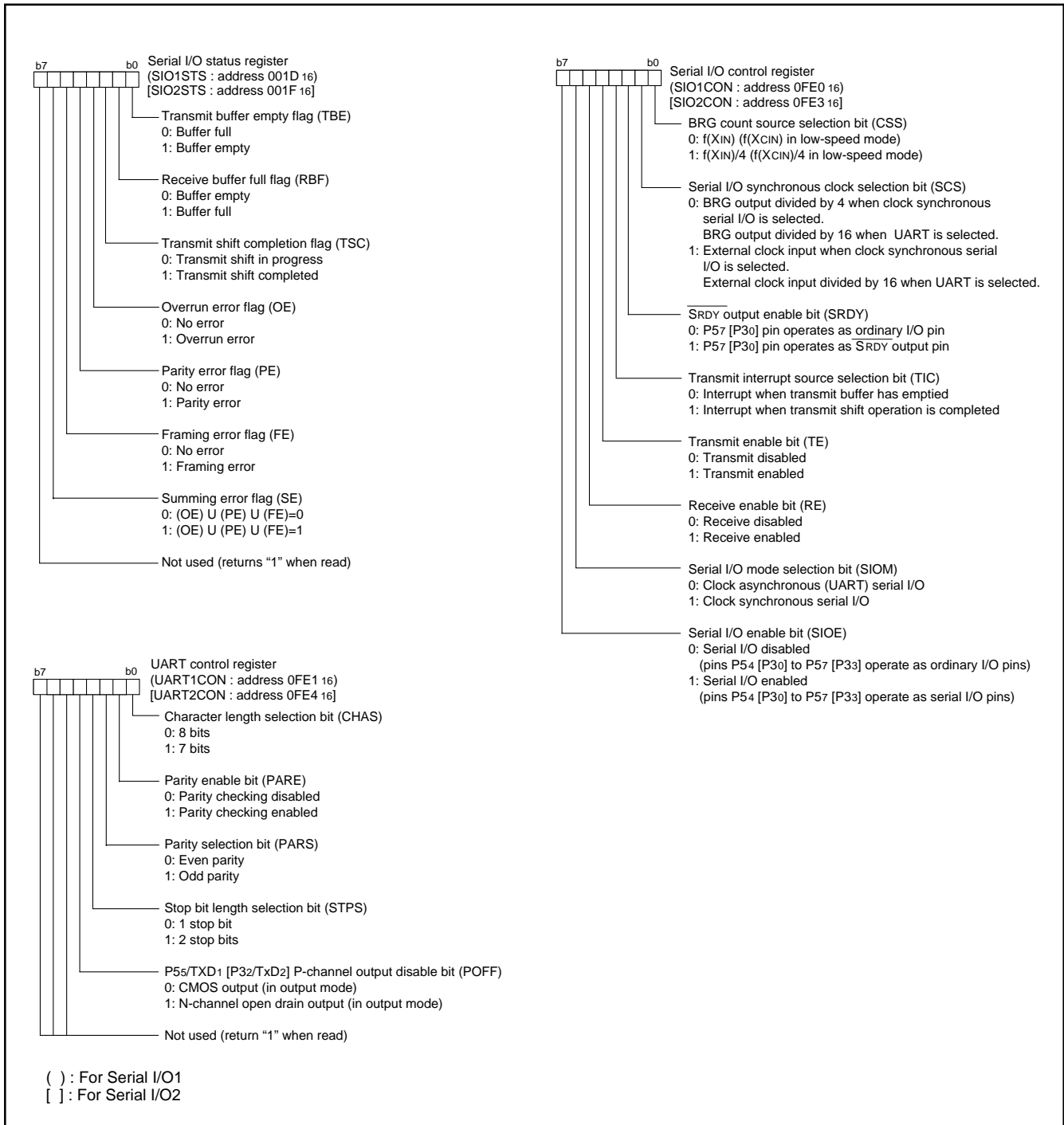


Fig. 29 Structure of serial I/O related registers

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

A-D CONVERTER

The 38C2 group has a 10-bit A-D converter. The A-D converter performs successive approximation conversion.

[A-D Conversion Register (ADL, ADH)]

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A-D conversion register (high-order) (address 001B16), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion register (low-order) (address 001A16).

During A-D conversion, do not read these registers. Also, the connection between the resistor ladder and reference voltage input pin (VREF) can be controlled by the VREF input switch bit (bit 0 of address 001A16). When "1" is written to this bit, the resistor ladder is always connected to VREF. When "0" is written to this bit, the resistor ladder is disconnected from VREF except during the A-D conversion.

[A-D Control Register (ADCON)]

This register controls A-D converter. Bits 2 to 0 are analog input pin selection bits. Bit 3 is an AD conversion completion bit and "0" during A-D conversion. This bit is set to "1" upon completion of A-D conversion. A-D conversion is started by setting "0" in this bit.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AVSS and VREF, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports P47/AN7–P40/AN0 and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1."

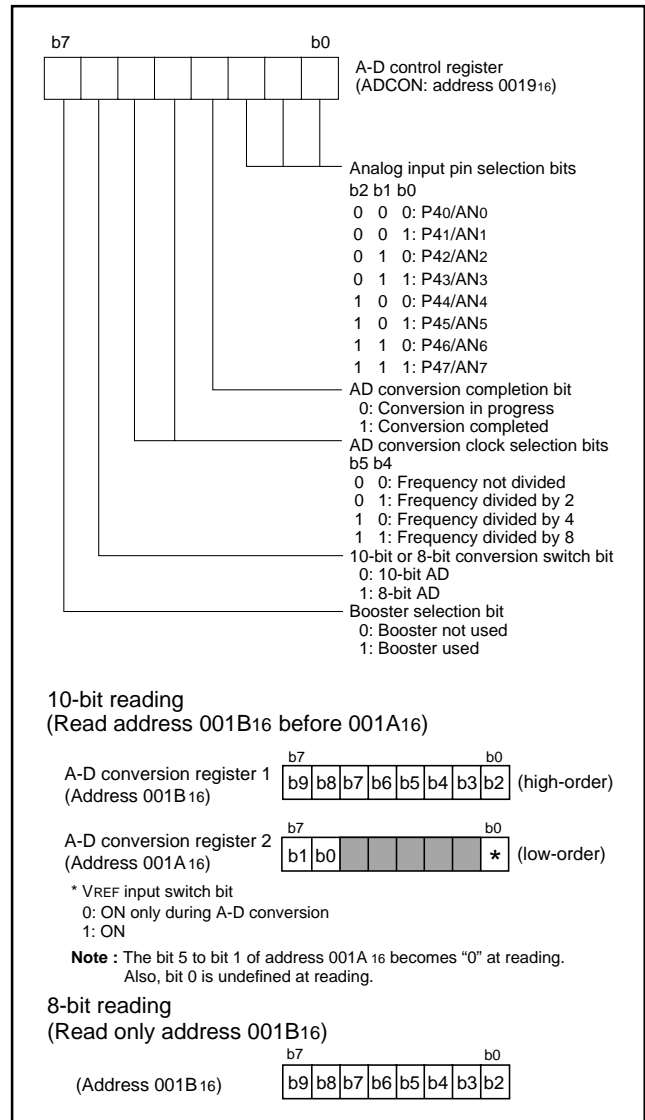


Fig. 30 Structure of A-D control register

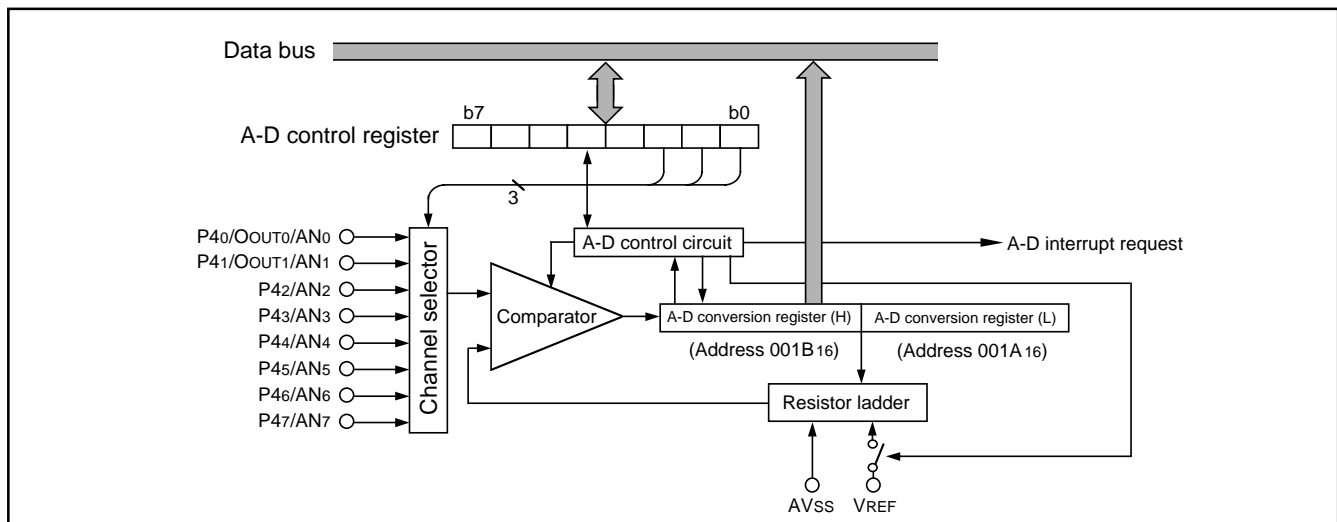


Fig. 31 Block diagram of A-D converter

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

LCD DRIVE CONTROL CIRCUIT

The 38C2 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output disable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 24 segment output pins and 4 common output pins can be used.

Up to 96 pixels can be controlled for an LCD display. When the LCD enable bit is set to "1" after data is set in the LCD mode register, the

segment output disable register, and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 8 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixels
2	48 dots or 8 segment LCD 6 digits
3	72 dots or 8 segment LCD 9 digits
4	96 dots or 8 segment LCD 12 digits

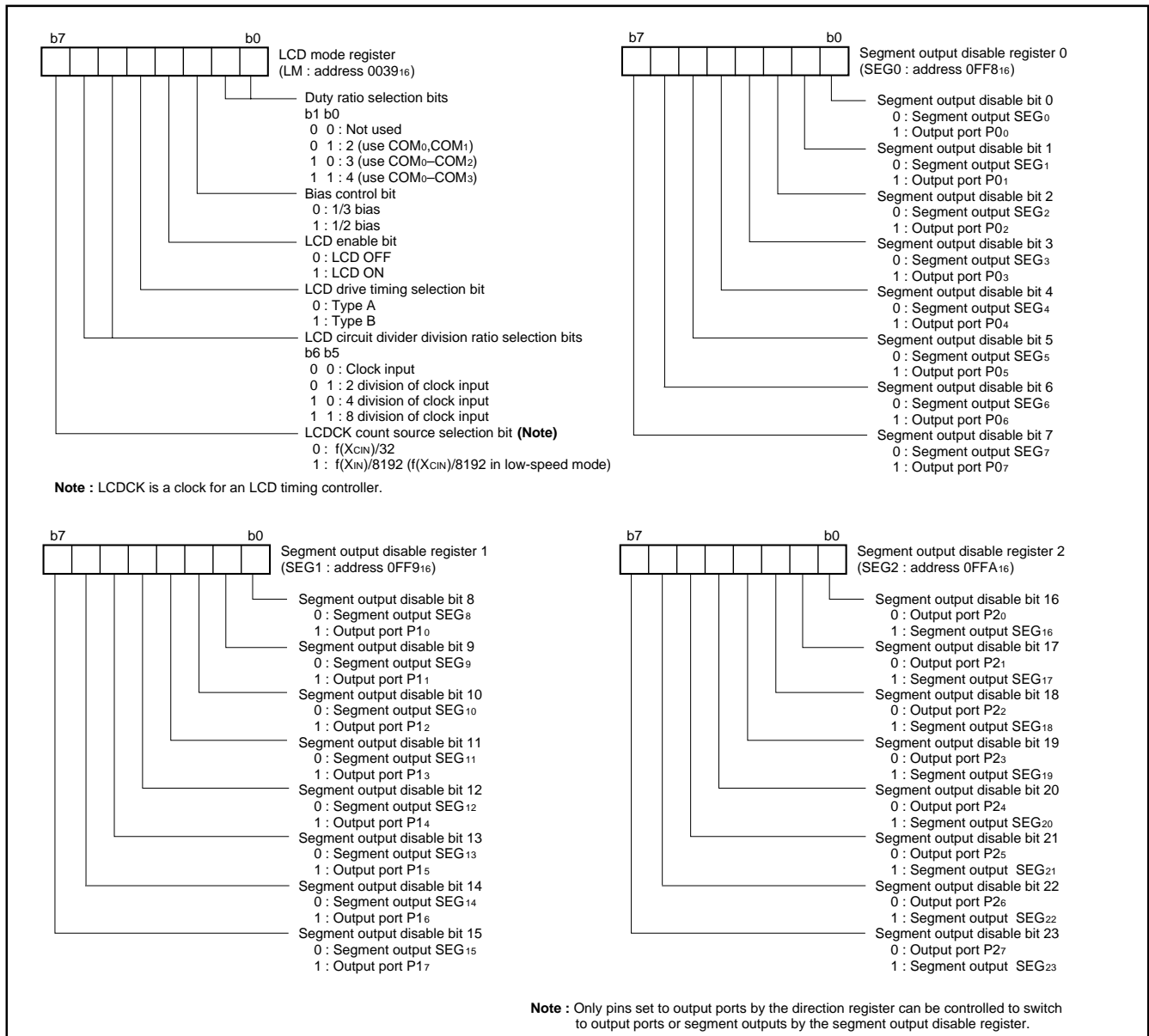


Fig. 32 Structure of LCD related registers

PRELIMINARY
 Notice: This is not a final specification.
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Bias Control and Applied Voltage to LCD Power Input Pins

When the voltage is applied from the LCD power input pins (VL1–VL3), set the VL pin input selection bit (bit 5 of the LCD power control register) and VL3 connection bit (bit 6 of LCD power control register) to “1”, apply the voltage value shown in Table 9 according to the bias value. In this case, SEG22 pin and SEG23 pin cannot be used. Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Table 9 Bias control and applied voltage to VL1–VL3

Bias value	Voltage value
1/3 bias	VL3=VLCD VL2=2/3 VLCD VL1=1/3 VLCD
1/2 bias	VL3=VLCD VL2=VL1=1/2 VLCD

Note : VLCD is the maximum value of supplied voltage for the LCD panel.

Common Pin and Duty Ratio Control

The common pins (COM0–COM3) to be used are determined by duty ratio. Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register). When reset is released, VCC voltage is output from the common pin.

Table 10 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
2	0	1	COM0, COM1
3	1	0	COM0–COM2
4	1	1	COM0–COM3

Note: Unused common pin outputs the unselected waveform.

Segment Signal Output Pin

The segment signal output pins (SEG0–SEG23) are shared with ports P0–P2. When these pins are used as the segment signal output pins, set the direction registers of the corresponding pins to “1”, and clear the segment output disable register to “0”.

Also, these pins are set to the input port after reset, the VCC voltage is output by the pull-up resistor.

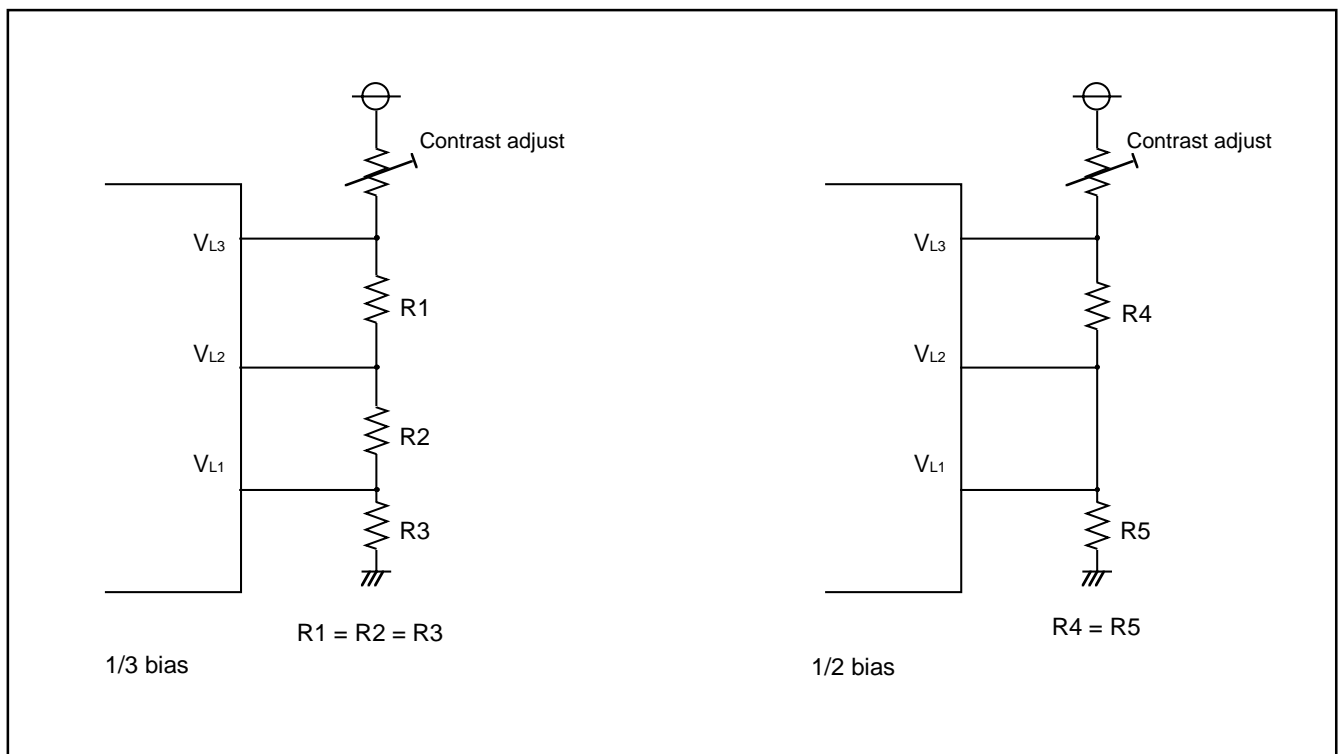


Fig. 34 Example of circuit at each bias (at external power input)

LCD Power Circuit

The LCD power circuit has the dividing resistor for LCD power which can be connected/disconnected with the LCD power control register.

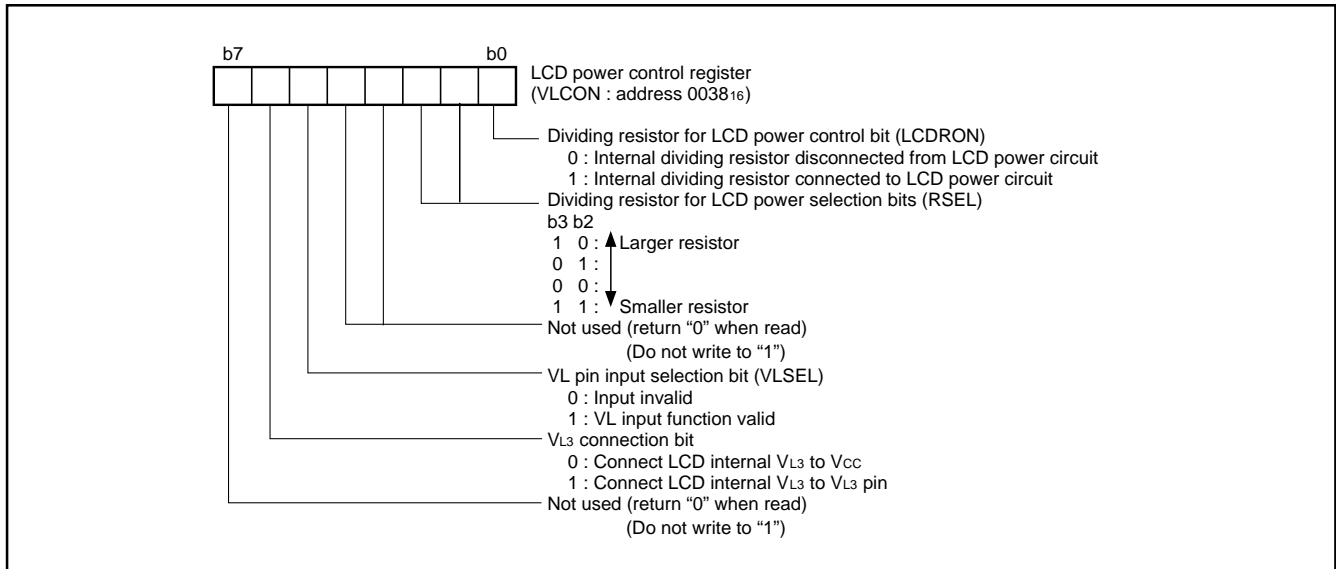


Fig. 35 Structure of LCD power control register

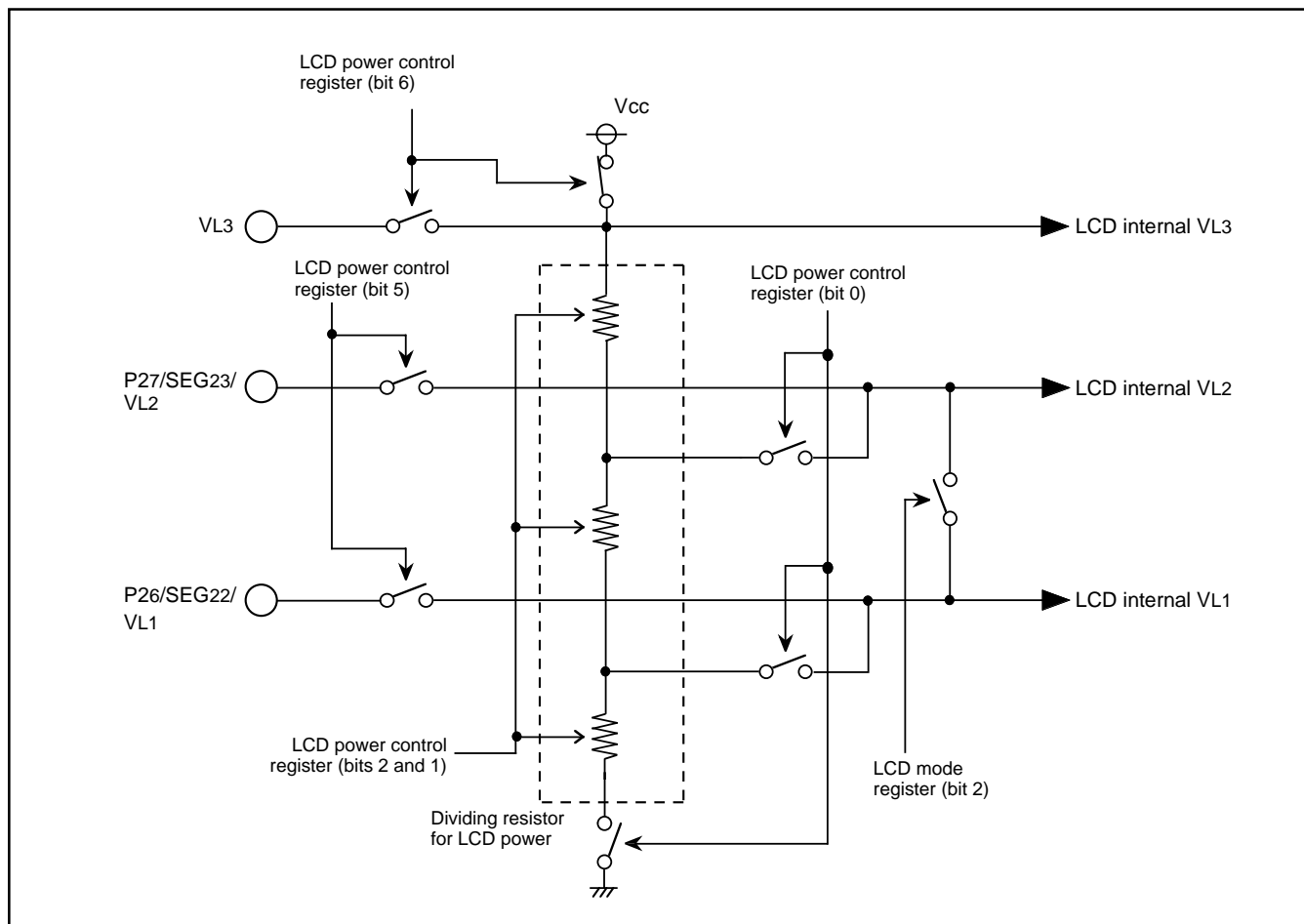


Fig. 36 VL block diagram

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

LCD Display RAM

The 12-byte area of address 0040₁₆ to 004B₁₆ is the designated RAM for the LCD display. When "1" is written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

For the LCD drive timing, type A or type B can be selected. The LCD drive timing is selected by the timing selection bit (bit 4 of LCD mode register). Type A is selected by setting the LCD drive timing selection bit to "0", type B is selected by setting the bit to "1". Type A is selected after reset.

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{duty ratio}}$$

■ Note

- (1) When the STP instruction is executed, the following bits are cleared to "0";
 - LCD enable bit (bit 3 of LCD mode register)
 - Bits other than bit 6 of the LCD power control register.
- (2) When the voltage is applied to VL1 to VL3 by using the external resistor, write "102" to dividing resistor for LCD power selection bits (RSEL) of the LCD power control register (address 38₁₆).

Bit Address	7	6	5	4	3	2	1	0
0040 ₁₆	SEG1			SEG0				
0041 ₁₆	SEG3			SEG2				
0042 ₁₆	SEG5			SEG4				
0043 ₁₆	SEG7			SEG6				
0044 ₁₆	SEG9			SEG8				
0045 ₁₆	SEG11			SEG10				
0046 ₁₆	SEG13			SEG12				
0047 ₁₆	SEG15			SEG14				
0048 ₁₆	SEG17			SEG16				
0049 ₁₆	SEG19			SEG18				
004A ₁₆	SEG21			SEG20				
004B ₁₆	SEG23			SEG22				
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Fig. 37 LCD display RAM map

PRELIMINARY
 Notice: This is not a final specification.
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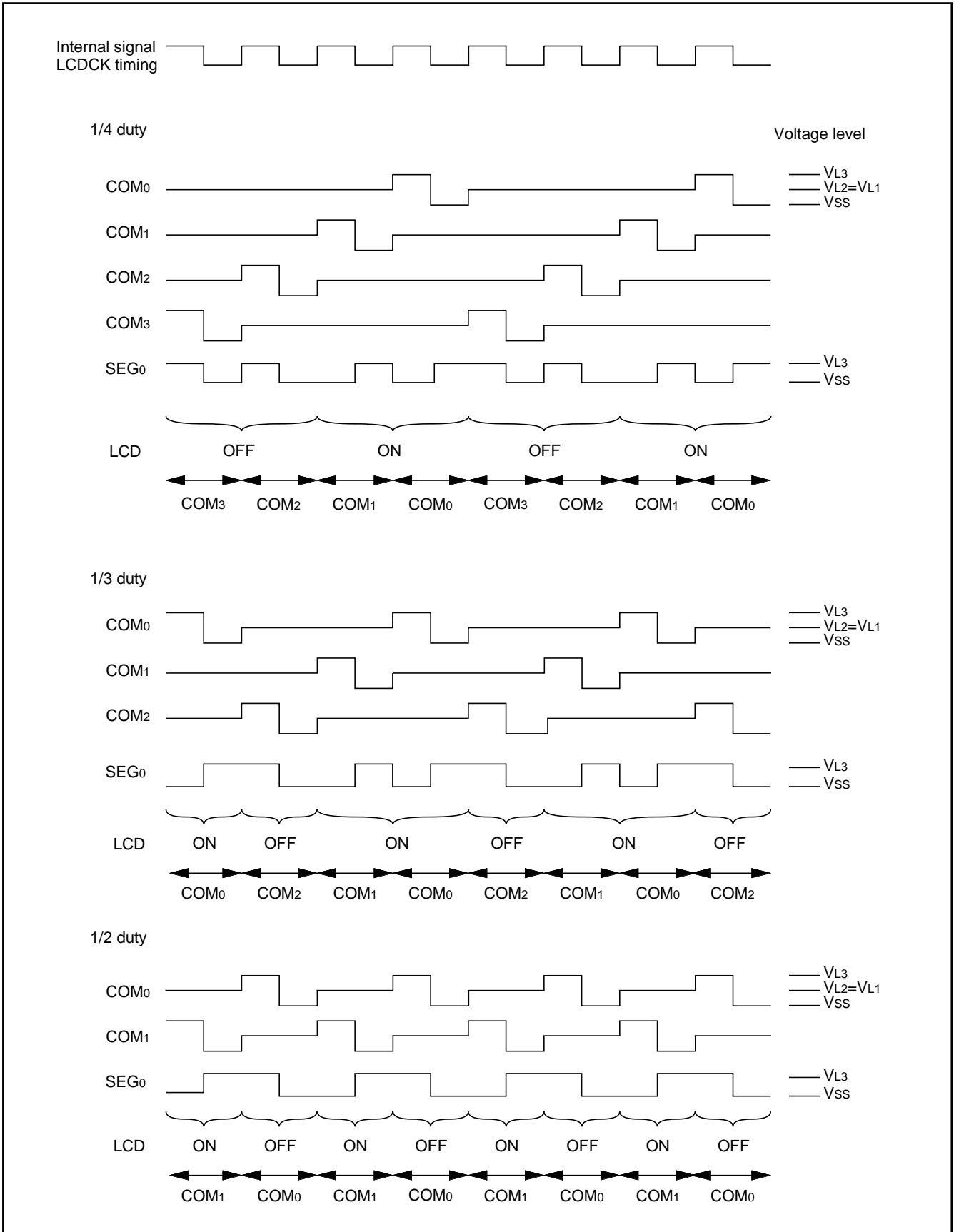


Fig. 38 LCD drive waveform (1/2 bias, type A)

PRELIMINARY
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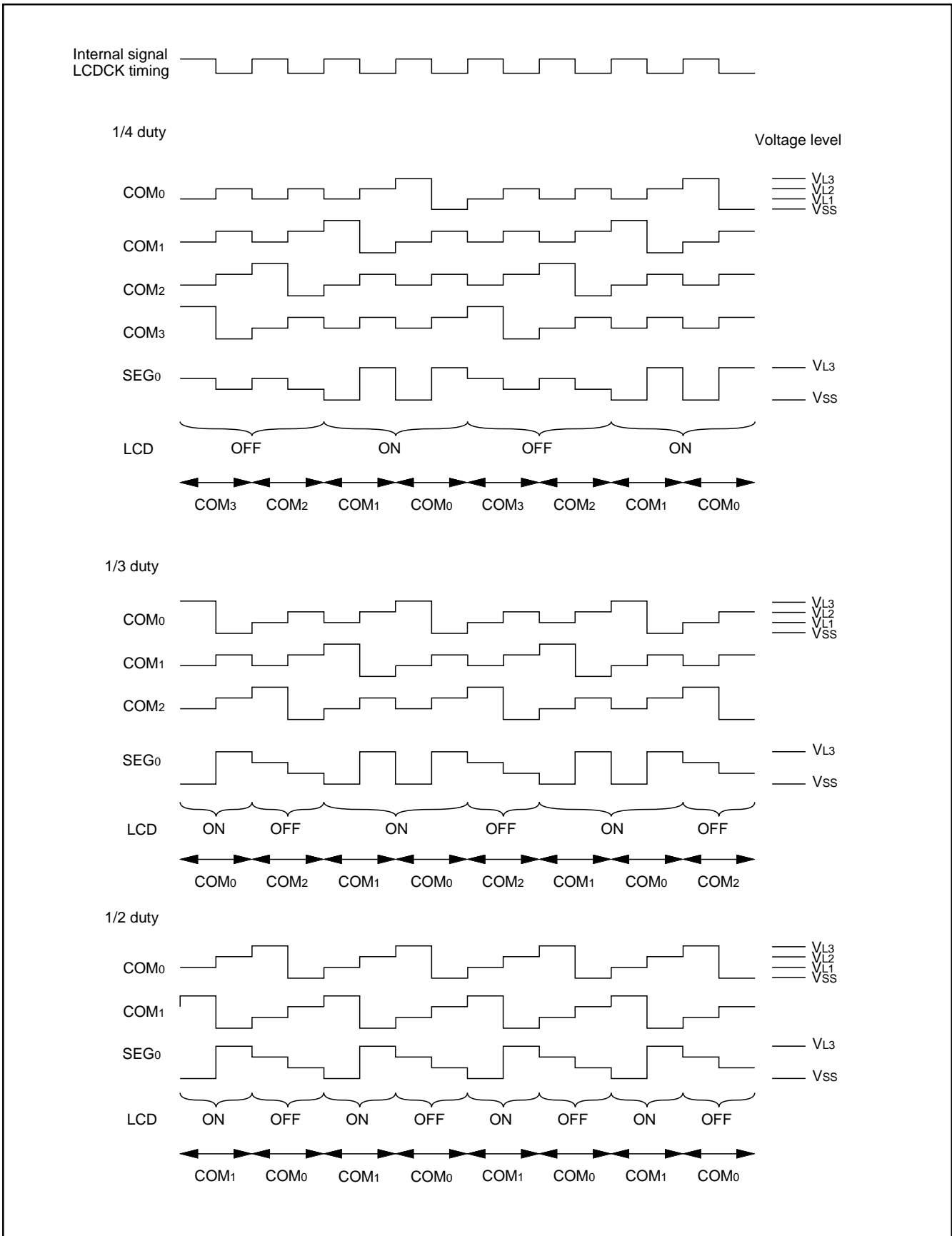


Fig. 39 LCD drive waveform (1/3 bias, type A)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

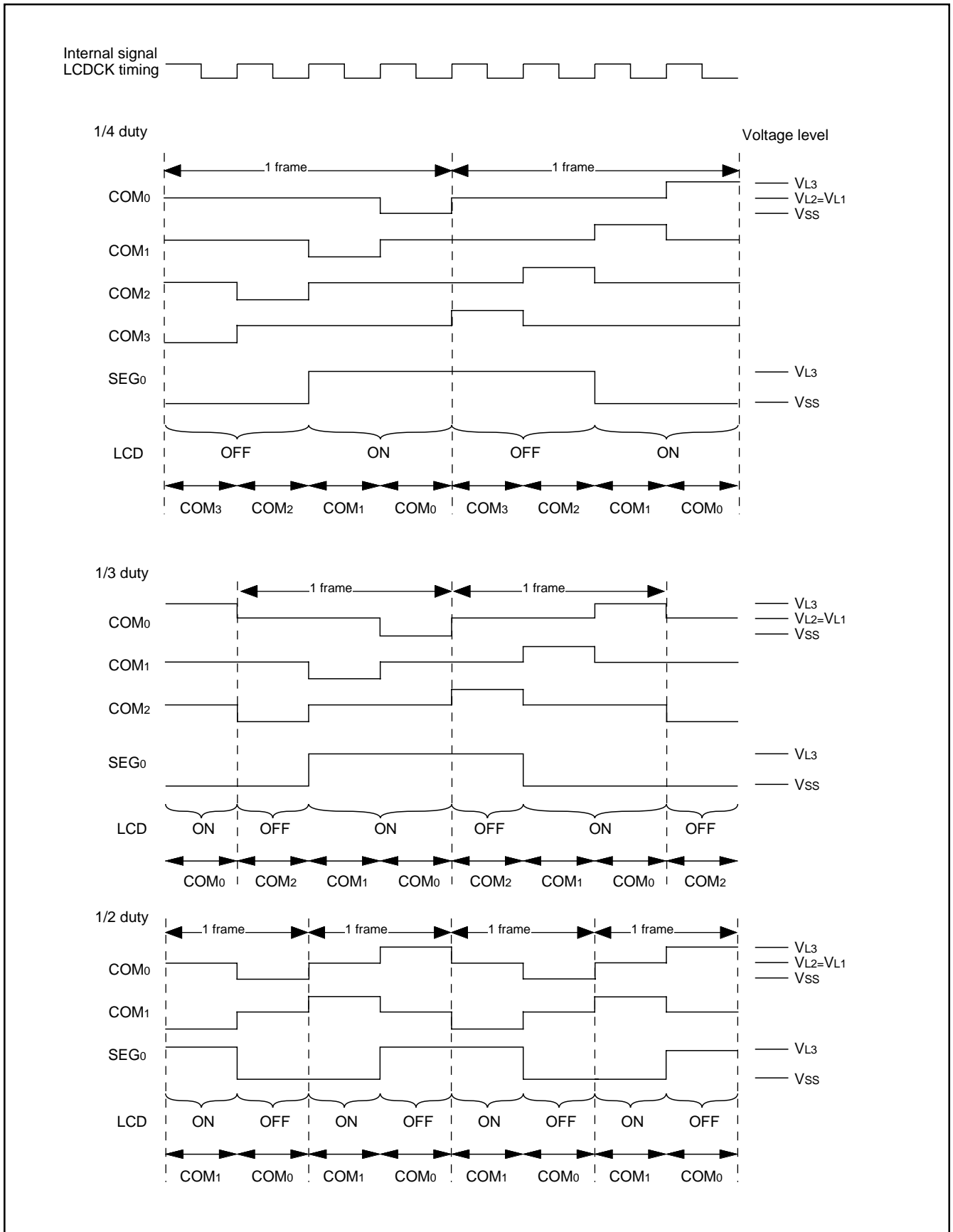


Fig. 40 LCD drive waveform (1/2 bias, type B)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

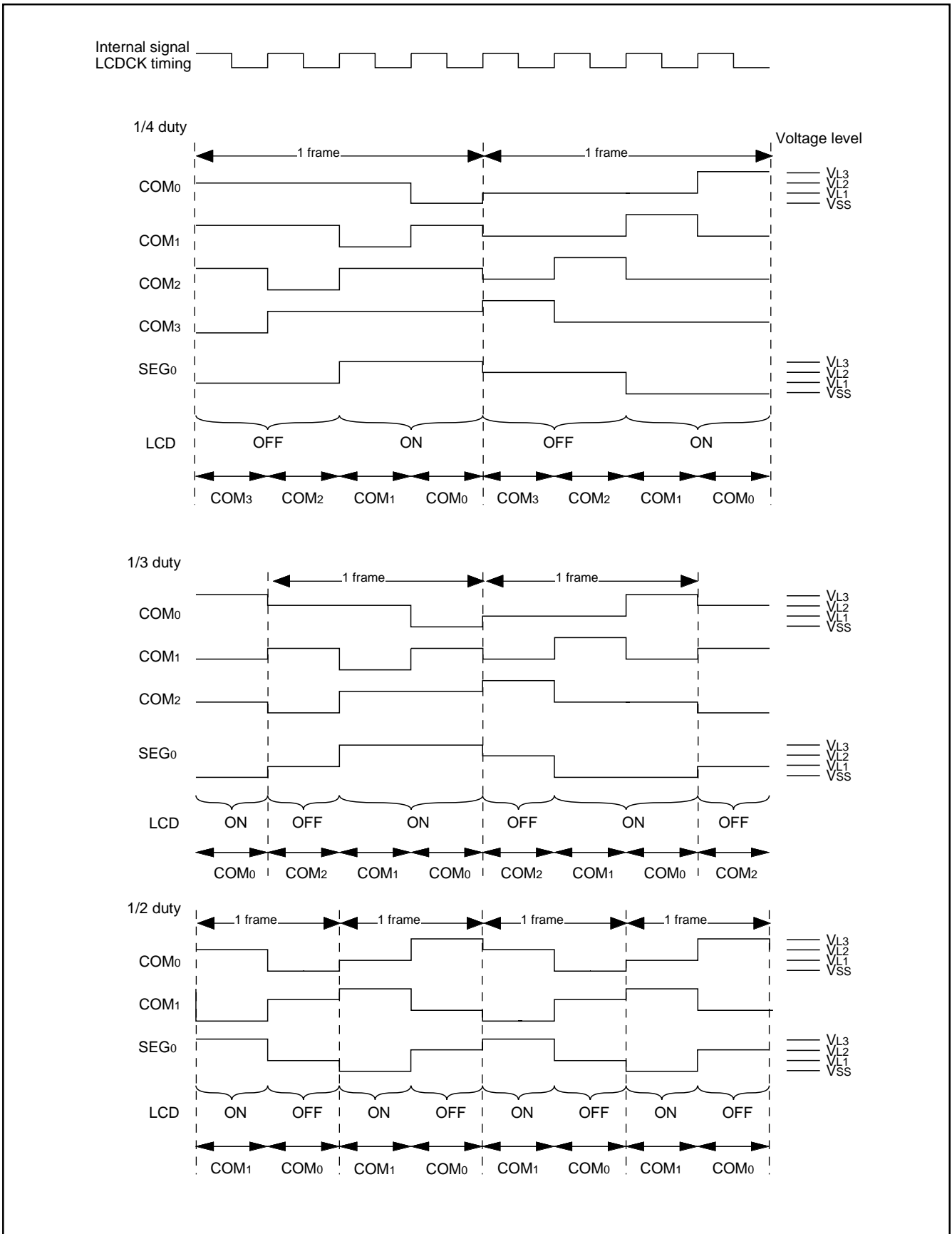


Fig. 41 LCD drive waveform (1/3 bias, type B)

CLOCK OUTPUT FUNCTION

A system clock ϕ can be output from I/O port P36. The triple function of I/O port, timer 2 output function and system clock ϕ output function is performed by the clock output control register (address 0018₁₆) and the timer 2 output selection bit of the timer 12 mode register (address 0025₁₆).

In order to output a system clock ϕ from I/O port P36, set the timer 2 output selection bit and bit 0 of the clock output control register to "1". When the clock output function is selected, a clock is output while the direction register of port P36 is set to the output mode. P36 is switched to the port output or the output (timer 2 output and the clock output) except port at the cycle after the timer 2 output control bit is switched.

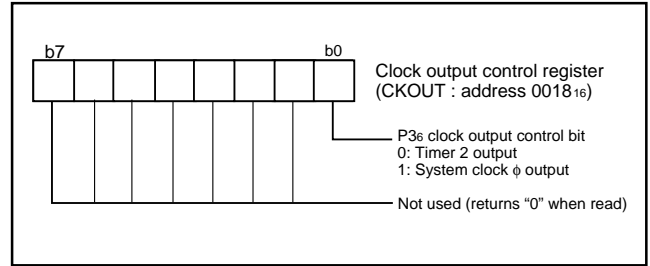


Fig. 45 Structure of clock output control register

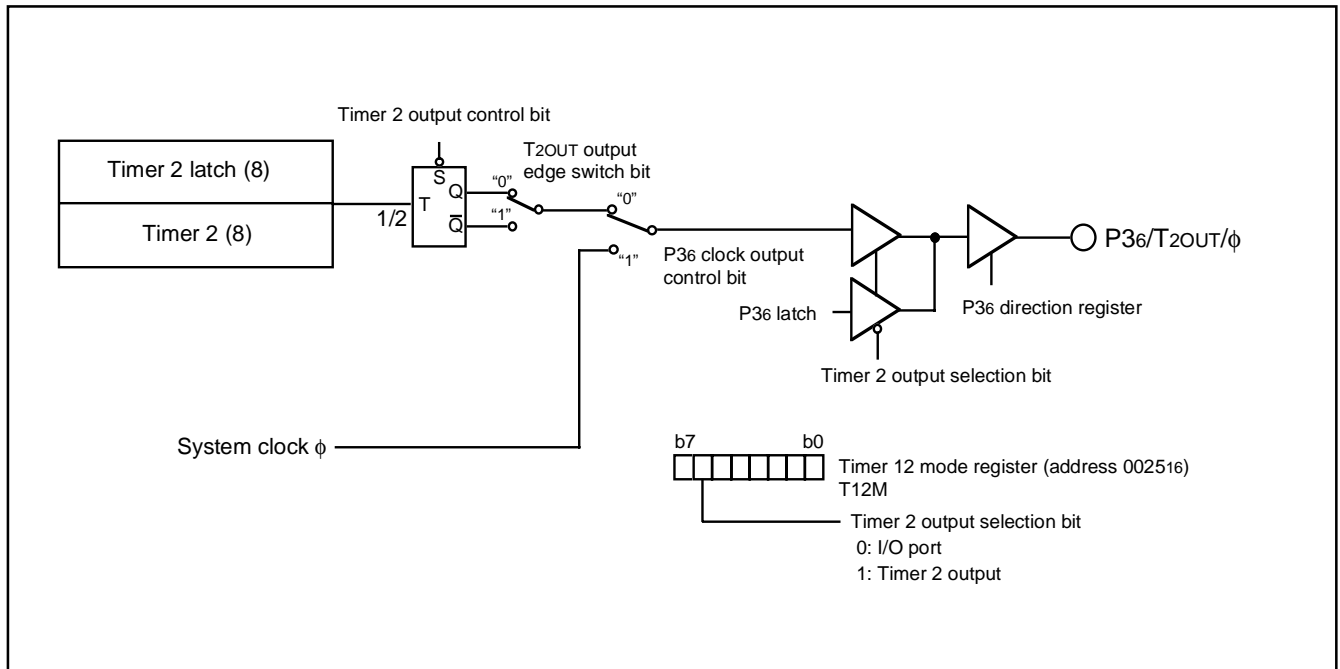


Fig. 46 Block diagram of Clock output function

PRELIMINARY
 Notice: This is not a final specification.
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RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between V_{CC} (min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address FFFD₁₆ (high-order byte) and address FFFC₁₆ (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. when a power source voltage passes V_{CC} (min.).

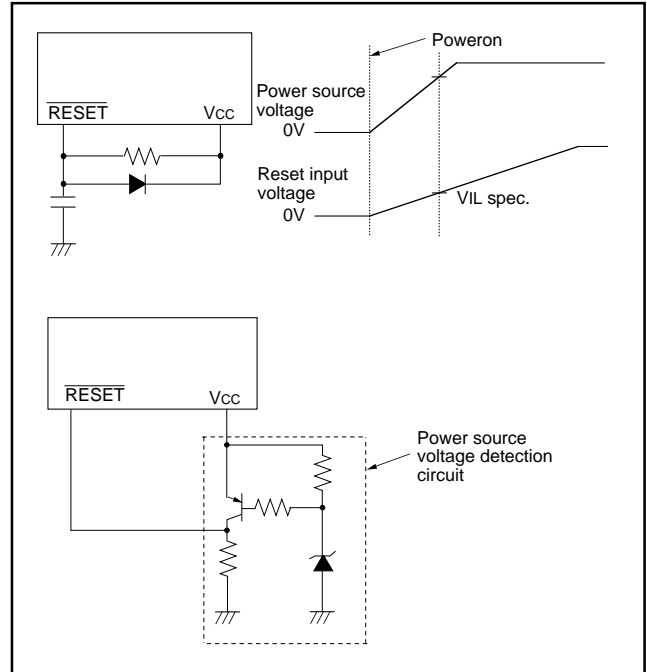


Fig. 47 Reset circuit example

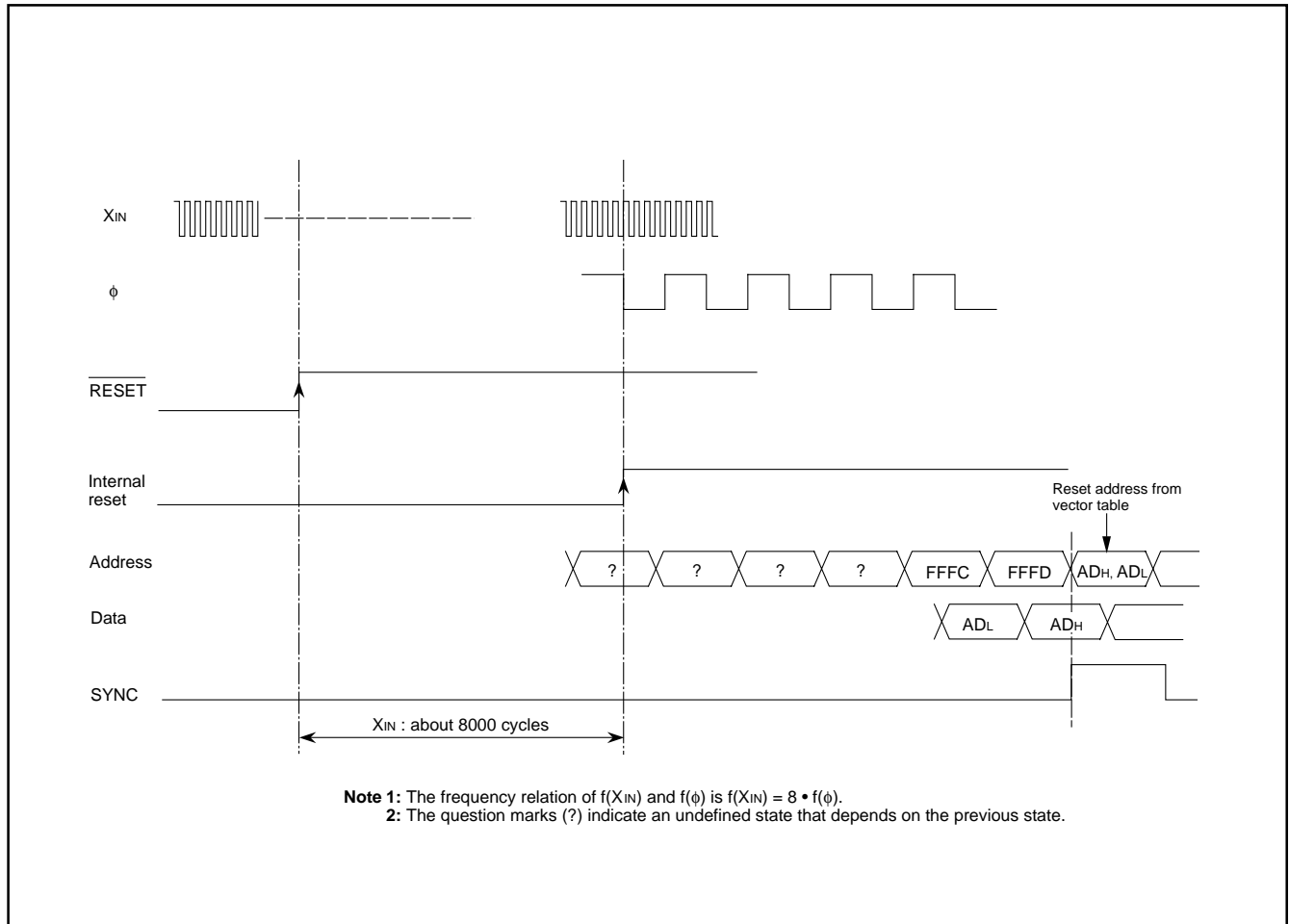


Fig. 48 Reset sequence

PRELIMINARY
 Notice: This is not a final specification.
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	Address	Register contents		Address	Register contents
(1) Port P0	0000 ₁₆	00 ₁₆	(35) Watchdog timer control register	0037 ₁₆	00111111
(2) Port P0 direction register	0001 ₁₆	00 ₁₆	(36) LCD power control register	0038 ₁₆	00 ₁₆
(3) Port P1	0002 ₁₆	00 ₁₆	(37) LCD mode register	0039 ₁₆	00 ₁₆
(4) Port P1 direction register	0003 ₁₆	00 ₁₆	(38) Interrupt edge selection register	003A ₁₆	00 ₁₆
(5) Port P2	0004 ₁₆	00 ₁₆	(39) CPU mode register	003B ₁₆	01001000
(6) Port P2 direction register	0005 ₁₆	00 ₁₆	(40) Interrupt request register 1	003C ₁₆	00 ₁₆
(7) Port P3	0006 ₁₆	00 ₁₆	(41) Interrupt request register 2	003D ₁₆	00 ₁₆
(8) Port P3 direction register	0007 ₁₆	00 ₁₆	(42) Interrupt control register 1	003E ₁₆	00 ₁₆
(9) Port P4	0008 ₁₆	00 ₁₆	(43) Interrupt control register 2	003F ₁₆	00 ₁₆
(10) Port P4 direction register	0009 ₁₆	00 ₁₆	(44) Serial I/O1 control register	0FE0 ₁₆	00 ₁₆
(11) Port P5	000A ₁₆	00 ₁₆	(45) UART1 control register	0FE1 ₁₆	11100000
(12) Port P5 direction register	000B ₁₆	00 ₁₆	(46) Serial I/O2 control register	0FE3 ₁₆	00 ₁₆
(13) Port P6	000C ₁₆	00 ₁₆	(47) UART2 control register	0FE4 ₁₆	11100000
(14) Port P6 direction register	000D ₁₆	00 ₁₆	(48) Oscillation output control register	0FF0 ₁₆	00 ₁₆
(15) Clock output control register	0018 ₁₆	00 ₁₆	(49) PULL register	0FF1 ₁₆	00 ₁₆
(16) A-D control register	0019 ₁₆	08 ₁₆	(50) Key input control register	0FF2 ₁₆	00 ₁₆
(17) Serial I/O1 status register	001D ₁₆	10000000	(51) Timer 1234 mode register	0FF3 ₁₆	00 ₁₆
(18) Serial I/O2 status register	001F ₁₆	10000000	(52) Timer X control register	0FF4 ₁₆	00 ₁₆
(19) Timer 1	0020 ₁₆	FF ₁₆	(53) Timer 12 frequency division selection register	0FF5 ₁₆	00 ₁₆
(20) Timer 2	0021 ₁₆	01 ₁₆	(54) Timer 34 frequency division selection register	0FF6 ₁₆	00 ₁₆
(21) Timer 3	0022 ₁₆	FF ₁₆	(55) Timer XY frequency division selection register	0FF7 ₁₆	00 ₁₆
(22) Timer 4	0023 ₁₆	FF ₁₆	(56) Segment output disable register 0	0FF8 ₁₆	FF ₁₆
(23) PWM01 register	0024 ₁₆	00 ₁₆	(57) Segment output disable register 1	0FF9 ₁₆	FF ₁₆
(24) Timer 12 mode register	0025 ₁₆	00 ₁₆	(58) Segment output disable register 2	0FFA ₁₆	FF ₁₆
(25) Timer 34 mode register	0026 ₁₆	00 ₁₆	(59) Timer Y mode register 2	0FFB ₁₆	00 ₁₆
(26) Compare register (low-order)	0028 ₁₆	00 ₁₆	(60) Flash memory control register	0FFE ₁₆	XXXX0001
(27) Compare register (high-order)	0029 ₁₆	00 ₁₆	(61) Processor status register	(PS)	XXXXX1XX
(28) Timer X (low-order)	002A ₁₆	FF ₁₆	(62) Program counter	(PC _H)	FFFD ₁₆ contents
(29) Timer X (high-order)	002B ₁₆	FF ₁₆		(PC _L)	FFFC ₁₆ contents
(30) Timer X (extension)	002C ₁₆	00 ₁₆			
(31) Timer Y (low-order)	002D ₁₆	FF ₁₆			
(32) Timer Y (high-order)	002E ₁₆	FF ₁₆			
(33) Timer X mode register	002F ₁₆	00 ₁₆			
(34) Timer Y mode register	0030 ₁₆	00 ₁₆			

X: Not fixed
 Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 49 Internal status at reset

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

CLOCK GENERATING CIRCUIT

The 38C2 group has two built-in oscillation circuits; main clock XIN–XOUT and sub-clock XCIN–XCOUT. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer’s recommended values. No external resistor is needed between XIN and XOUT since a feedback resistor exists on-chip. However, an external feedback resistor is needed between XCIN and XCOUT.

When the clock signal is supplied from external for the main clock, input the signal to XIN pin and input the inverted-phase signal of XIN to XOUT pin by the external inverter.

When the clock signal is supplied from external for the sub-clock, input the signal to XCIN and leave XCOUT open.

Immediately after power on, only the XIN oscillation circuit starts oscillating.

Frequency Control

(1) Frequency/8 Mode

The system clock ϕ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) Frequency/4 Mode

The system clock ϕ is the frequency of XIN divided by 4.

(3) Frequency/2 Mode

The system clock ϕ is the frequency of XIN divided by 2.

(4) Through Mode

The system clock ϕ is the frequency of XIN.

(5) Low-speed Mode

The system clock ϕ is the frequency of XCIN divided by 2. In the low-speed mode, the low-power dissipation operation can be performed when the main clock XIN is stopped by setting the bit 7 of the CPU mode register to “0”. In this case, when main clock XIN oscillation is restarted, generate the wait time until the oscillation is stable by program after the bit 7 of the CPU mode register is set to “1”.

Notes on Clock Generating Circuit

If you switch the mode between through, frequency/2/4, or 8 and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode, set the frequency on condition that $f(XIN) > 3f(XCIN)$.

Oscillation Control

(1) Stop Mode

If the STP instruction is executed, the system clock ϕ stops at an “H” level, and main clock and sub-clock oscillators stop.

In this time, values set previously to timer 1 latch and timer 2 latch are loaded automatically to timer 1 and timer 2. Set the values to generate the wait time required for oscillation stabilization to timer 1 latch and timer 2 latch (low-order 8 bits of timer 1 and high-order 8 bits of timer 2) before the STP instruction.

The frequency divider for timer 1 is used for the timer 1 count source, and the output of timer 1 is forcibly connected to timer 2. In this time, bits 0 to 5 of the timer 12 mode register are cleared to “0”.

The values of the timer 12 frequency divider selection register are not changed.

Set the interrupt enable bits of the timer 1 and timer 2 to disabled (“0”) before executing the STP instruction.

Oscillator restarts When reset occurs or an interrupt request is received, but the system clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait Mode

If the WIT instruction is executed, the system clock ϕ stops at an “H” level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The system clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

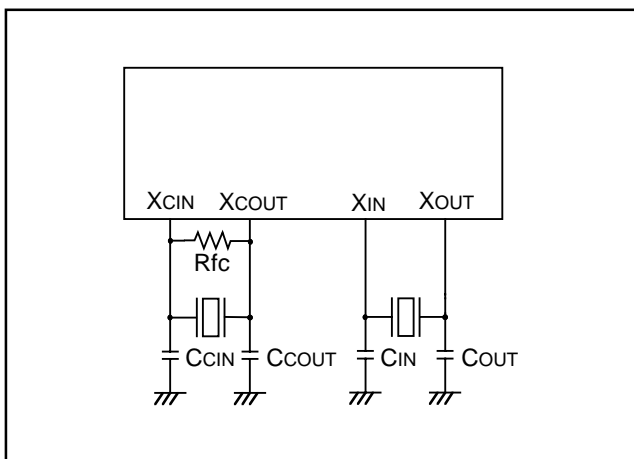


Fig. 50 Ceramic resonator circuit

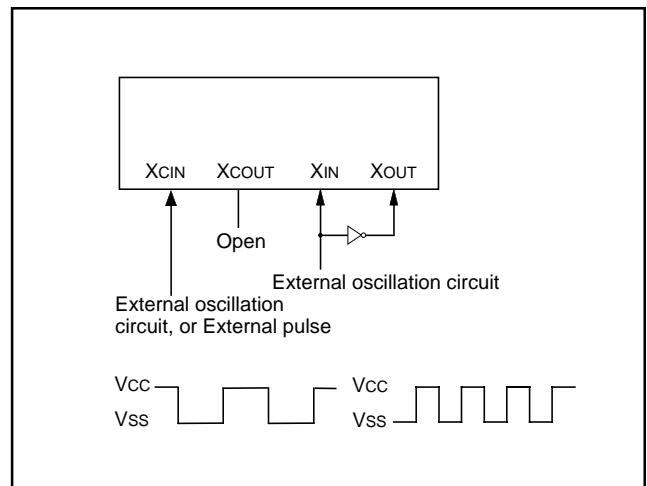


Fig. 51 External clock input circuit

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

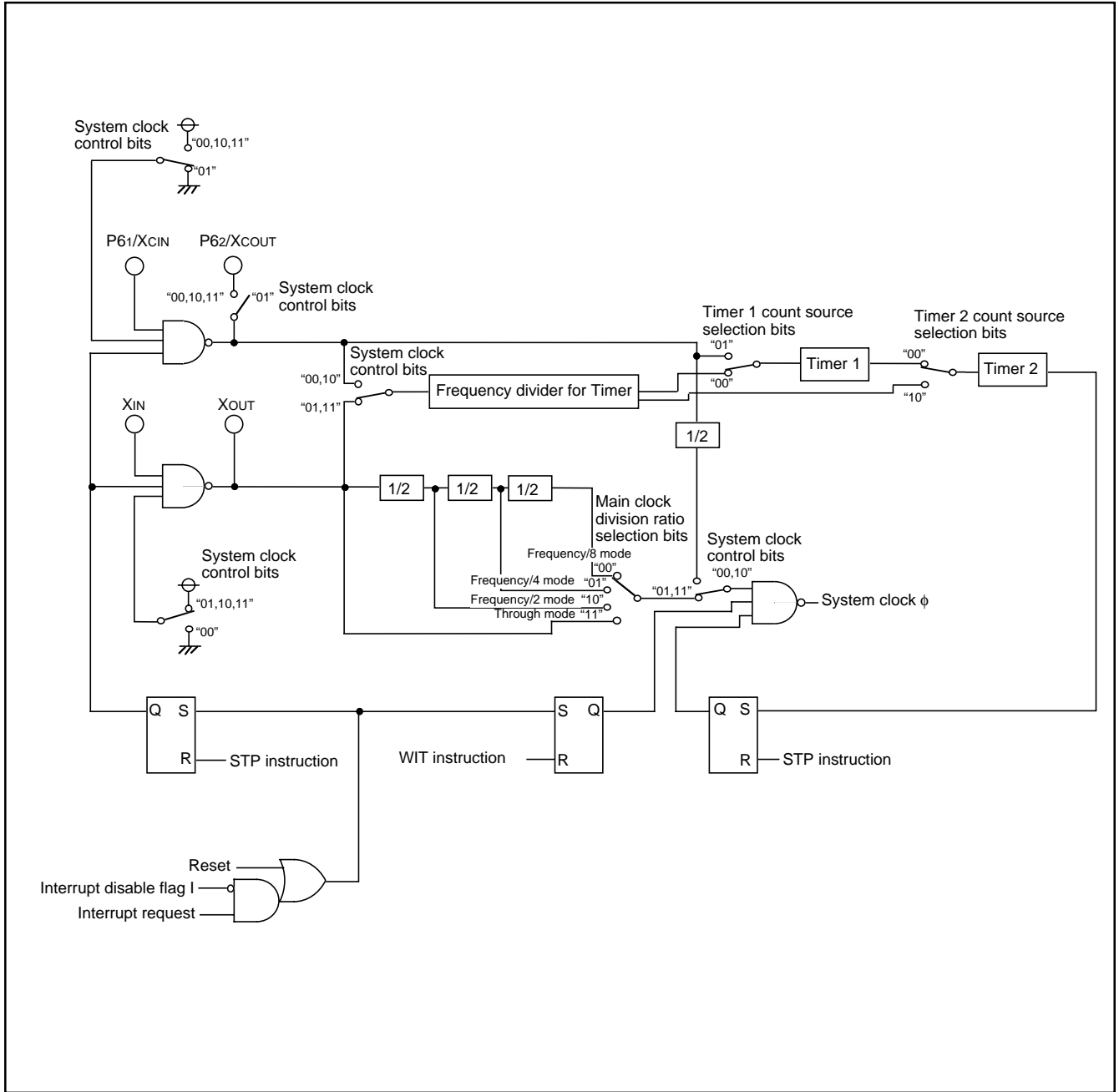
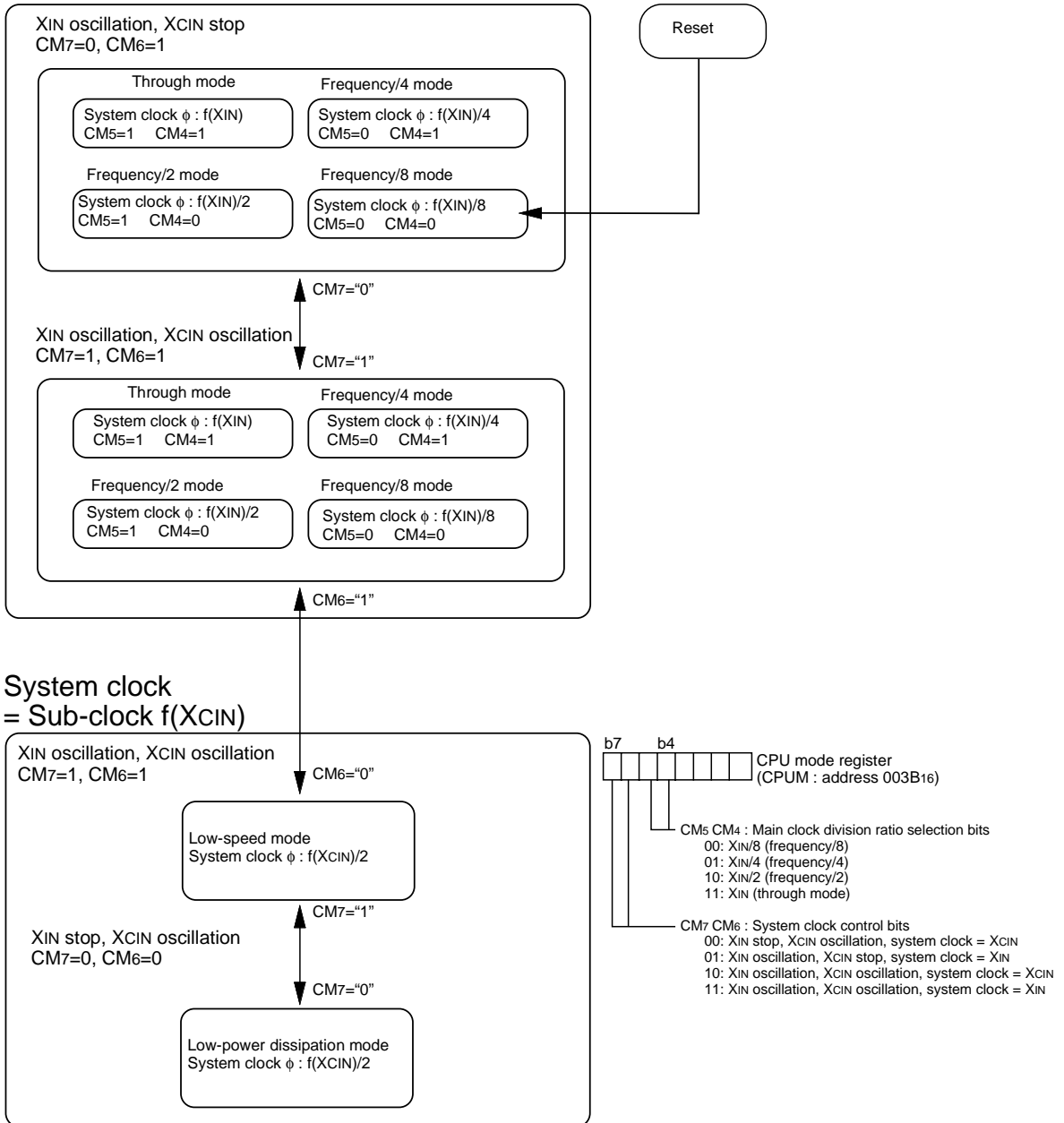


Fig. 52 Clock generating circuit block diagram

System clock = Main clock $f(XIN)$



- Notes**
- 1: When the mode is switched from through or frequency/2/4/8 to the low-speed mode, or the opposite is performed, change CM7 at first, and then, change CM6 after the oscillation of the changed mode is stabilized.
 - 2: The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
 - 3: Timer and LCD operate in the wait mode.
 - 4: When the stop mode is ended, a delay time can be set by connecting timer 1 and timer 2.

Fig. 53 State transitions of system clock

Oscillation External Output Function

The 38C2 group has the oscillation external output function to output the rectangular waveform of the clock obtained by the oscillation circuits from P41 and P40.

In order to validate the oscillation external output function, set P40 or P41, or both to the output mode (set the corresponding direction register to "1").

The level of the XCOUT external output signal becomes "H" by the P40/P41 oscillation output control bits (bits 0 and 1) of the oscillation output control register (address 0FF0₁₆) in the following states;

- the function to output the signal from the XCOUT pin externally is selected
 - the sub-clock (XCIN–XCOUT) is in the oscillating or stop mode.
- Likewise, the level of the XOUT external output signal becomes "H" by the P40/P41 oscillation output control bits (bits 0 and 1) of the oscillation output control register (address 0FF0₁₆) in the following states;
- the function to output the signal from the XOUT pin externally is selected
 - the main clock (XIN–XOUT) is in the oscillating or stop mode.

Note

When the signal from the XOUT pin or XCOUT pin of the oscillation circuit is input directly to the circuit except this MCU and used, the system operation may be unstabilized.

In order to share the oscillation circuit safely, use the clock output from P40 and P41 by this function for the circuits except this MCU.

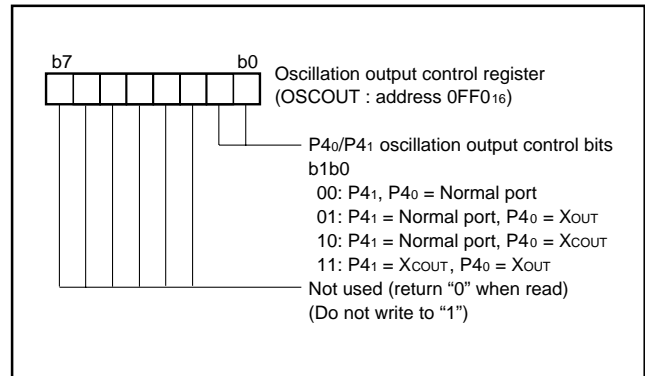


Fig. 54 Structure of oscillation output control register

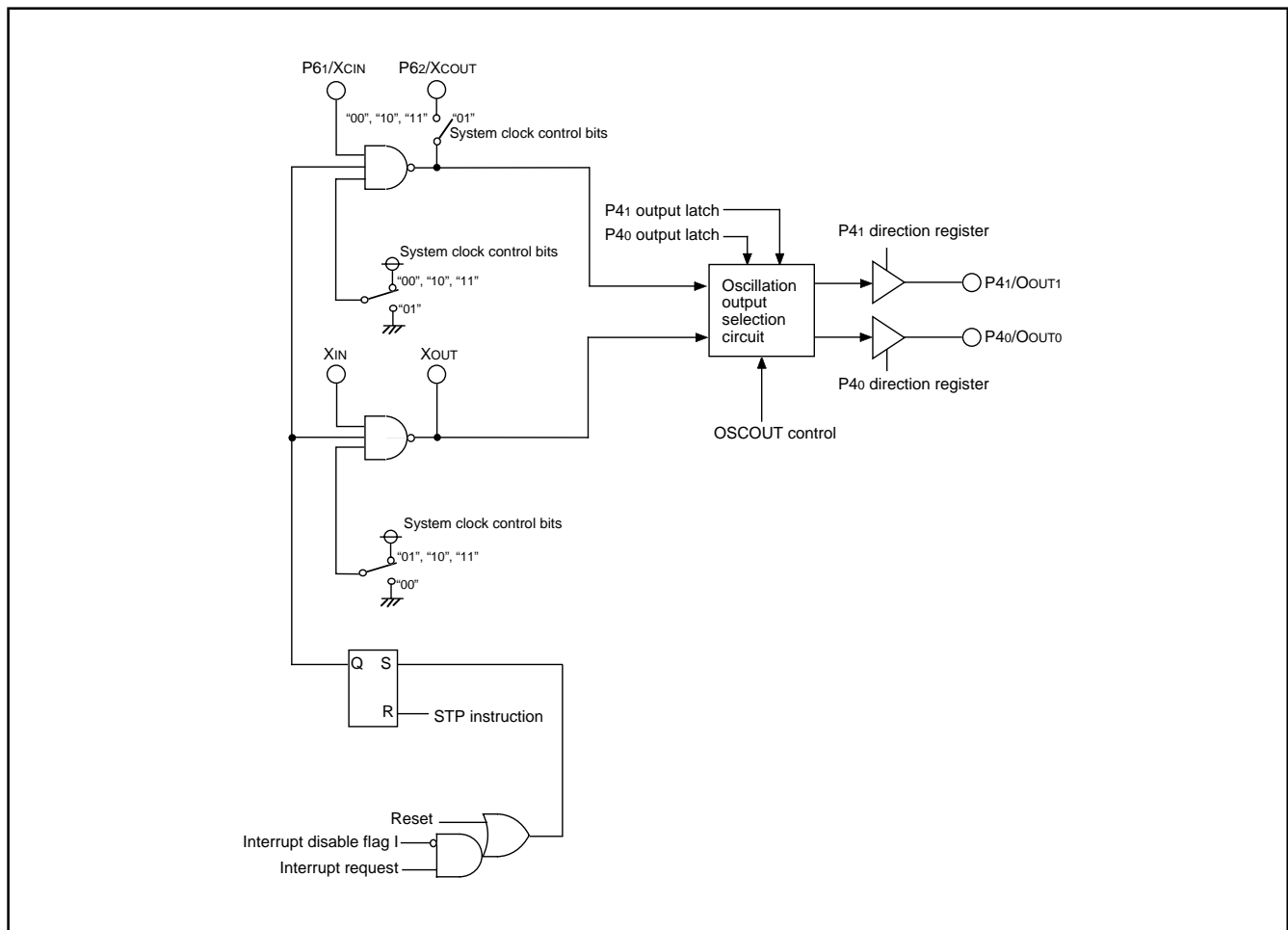


Fig. 55 Block diagram of Oscillation output function

PRELIMINARY
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NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1," then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing an SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- The timers share the one frequency divider to generate the count source. Accordingly, when each timer starts operating, initializing the frequency divider is not executed. Therefore, when the frequency divider is selected for the count source, the delay of the maximum one cycle of the count source is generated until the timer starts counting or the waveform is output from timer starts operating. Also, the count source cannot be checked externally.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1." Serial I/O continues to output the final bit from the TXD pin after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Therefore, make sure that $f(\text{XIN})$ is at least on 250 kHz (Note) during an A-D conversion.

Note: When the frequency divided by $2/4/8$ is selected by the AD conversion clock selection bits, the above frequency is multiplied by $2/4/8$. Also, when the STP instruction is executed during the A-D conversion, the A-D conversion is stopped immediately, the A-D conversion completion bit is set to "1", and the interrupt request is generated.

LCD

When the LCD power input pin VL3 is not used, connect it to Vcc.

Instruction Execution Time

The instruction execution time is obtained by multiplying the number of cycles shown in the list of machine instructions by the period of the internal clock ϕ .

PRELIMINARY
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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 11 Absolute maximum ratings (Mask ROM version)

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	All voltages are based on Vss. Output transistors are cut off.	-0.3 to 6.5	V
Vi	Input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P62		-0.3 to VCC+0.3	V
Vi	Input voltage VL1		-0.3 to VL2	V
Vi	Input voltage VL2		VL1 to VL3	V
Vi	Input voltage VL3		VL2 to 6.5	V
Vi	Input voltage RESET, XIN, CNVss		-0.3 to VCC+0.3	V
Vo	Output voltage P00-P07, P10-P17, P20-P27		At output port	-0.3 to VCC+0.3
		At segment output	-0.3 to VL3+0.3	V
Vo	Output voltage COM0-COM3		-0.3 to VL3+0.3	V
Vo	Output voltage P30-P37, P40-P47, P50-P57, P60-P62		-0.3 to VCC+0.3	V
Vo	Output voltage XOUT		-0.3 to VCC+0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-40 to 125	°C

Recommended Operating Conditions

Table 12 Recommended operating conditions (Mask ROM version)

(VCC = 1.8 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage	f(φ) = 8 MHz	4.0	5.0	5.5	V
		f(φ) = 2 MHz	1.8	5.0	5.5	V
		Low-speed mode	1.8	5.0	5.5	V
VSS	Power source voltage			0		V
VREF	A-D converter reference voltage		VCC-0.3		VCC+0.3	V
AVSS	Analog power source voltage			0		V
VIA	Analog input voltage AN0-AN7		AVSS		VCC	V
VIH	"H" input voltage	P04-P07, P10-P17, P20-P27, P30, P32, P35, P36, P40-P47, P52, P53, P62	0.7VCC		VCC	V
VIH	"H" input voltage	P00-P03, P31, P33, P34, P37, P50, P51, P54-P57, P60, P61	0.8VCC		VCC	V
VIH	"H" input voltage	RESET	2.2 V ≤ VCC ≤ 5.5 V	0.9VCC	VCC	V
			VCC ≤ 2.2 V	$VCC - \frac{65 \times VCC - 99}{100}$	VCC	
VIH	"H" input voltage	XIN, XCIN	1.5		VCC	V
VIL	"L" input voltage	P04-P07, P10-P17, P20-P27, P30, P32, P35, P36, P40-P47, P52, P53, P62	0		0.3VCC	V
VIL	"L" input voltage	P00-P03, P31, P33, P34, P37, P50, P51, P54-P57, P60, P61, CNVSS	0		0.2VCC	V
VIL	"L" input voltage	RESET	2.2 V ≤ VCC ≤ 5.5 V	0	0.2VCC	V
			VCC ≤ 2.2 V	0	$\frac{65 \times VCC - 99}{100}$	
VIL	"L" input voltage	XIN, XCIN	0		0.4	V

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Table 13 Recommended operating conditions

(V_{CC} = 1.8 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current (Note 1) P00-P07, P10-P17, P20-P27, P30-P37			-20	mA
ΣIOH(peak)	"H" total peak output current (Note 1) P40-P47, P50-P57, P60-P62			-20	mA
ΣIOL(peak)	"L" total peak output current (Note 1) P00-P07, P10-P17, P20-P27			20	mA
ΣIOL(peak)	"L" total peak output current (Note 1) P40-P47, P50, P51, P54-P57, P60-P62			20	mA
ΣIOL(peak)	"L" total peak output current (Note 1) P30-P37, P52, P53			110	mA
ΣIOH(avg)	"H" total average output current (Note 1) P00-P07, P10-P17, P20-P27, P30-P37			-10	mA
ΣIOH(avg)	"H" total average output current (Note 1) P40-P47, P50-P57, P60-P62			-10	mA
ΣIOL(avg)	"L" total average output current (Note 1) P00-P07, P10-P17, P20-P27			10	mA
ΣIOL(avg)	"L" total average output current (Note 1) P40-P47, P50, P51, P54-P57, P60-P62			10	mA
ΣIOL(avg)	"L" total average output current (Note 1) P30-P37, P52, P53			90	mA
IOH(peak)	"H" peak output current (Note 2) P00-P07, P10-P17, P20-P27			-1.0	mA
IOH(peak)	"H" peak output current (Note 2) P30-P37, P41-P47, P50-P57, P60-P62			-5.0	mA
IOL(peak)	"L" peak output current (Note 2) P00-P07, P10-P17, P20-P27			10	mA
IOL(peak)	"L" peak output current (Note 2) P40-P47, P50, P51, P54-P57, P60-P62			10	mA
IOL(peak)	"L" peak output current (Note 2) P30-P37, P52, P53			30	mA
IOH(avg)	"H" average output current (Note 3) P00-P07, P10-P17, P20-P27			-0.5	mA
IOH(avg)	"H" average output current (Note 3) P40-P47, P50-P57, P60-P62			-2.5	mA
IOL(avg)	"L" average output current (Note 3) P00-P07, P10-P17, P20-P27			5.0	mA
IOL(avg)	"L" average output current (Note 3) P40-P47, P50, P51, P54-P57, P60-P62			5.0	mA
IOL(avg)	"L" average output current (Note 3) P30-P37, P52, P53			15	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is average value measured over 100 ms.

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Table 14 Recommended operating conditions (Mask ROM version)

(V_{CC} = 1.8 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0)	Timer X and Timer Y	(4.0 V ≤ V _{CC} ≤ 5.5 V)			4.0	MHz
f(CNTR1)	Input frequency (duty cycle 50%)	(V _{CC} ≤ 4.0 V)			(15×V _{CC} -16)/11	MHz
f(φ)	System clock φ frequency	(4.0 V ≤ V _{CC} ≤ 5.5 V)			8.0	MHz
		(V _{CC} ≤ 4.0 V)			(30×V _{CC} -32)/11	MHz
f(XIN)	Main clock input oscillation frequency (Note 1)	(2.0 V ≤ V _{CC} ≤ 5.5 V)			8.0	MHz
		(V _{CC} ≤ 2.0 V)			20×V _{CC} -32	MHz
f(XCIN)	Sub-clock input oscillation frequency (Notes 1, 2)		32.768		50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

Electrical Characteristics

Table 15 Electrical characteristics (Mask ROM version)

(V_{CC} = 4.0 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	“H” output voltage P00-P07, P10-P17, P20-P27	I _{OH} = -1 mA	V _{CC} -2.0			V
		I _{OH} = -0.25 mA	V _{CC} -0.8			V
		V _{CC} = 1.8 V				
VOH	“H” output voltage P30-P37, P40-P47, P50-P57, P60-P62	I _{OH} = -5 mA	V _{CC} -2.0			V
		I _{OH} = -1.5 mA	V _{CC} -0.5			V
		I _{OH} = -1.25 mA	V _{CC} -0.8			V
		V _{CC} = 1.8 V				
VOL	“L” output voltage P00-P07, P10-P17, P20-P27, P40-P47, P50, P51, P54-P57, P60-P62	I _{OL} = 10 mA			2.0	V
		I _{OL} = 3 mA			0.5	V
		I _{OL} = 2.5 mA			0.8	V
		V _{CC} = 1.8 V				
VOL	“L” output voltage P30-P37, P52, P53	I _{OL} = 15 mA			2.0	V
		I _{OL} = 4 mA			0.8	V
		V _{CC} = 1.8 V				
VT+–VT-	Hysteresis INT0–INT2, CNTR0, CNTR1, P00–P03, P54–P57			0.5		V
VT+–VT-	Hysteresis SCLK1, SCLK2, RxD1, RxD2			0.5		V
VT+–VT-	Hysteresis RESET			0.5		V
I _{IH}	“H” input current P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P62	V _I = V _{CC}			5.0	μA
I _{IH}	“H” input current RESET	V _I = V _{CC}			5.0	μA
I _{IH}	“H” input current XIN	V _I = V _{CC}		4.0		μA
I _{IL}	“L” input current P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P62	V _I = V _{SS} Pull-up “OFF”			-5.0	μA
		V _{CC} = 5.0 V, V _I = V _{SS} Pull-up “ON”	-60	-120	-240	μA
		V _{CC} = 1.8 V, V _I = V _{SS} Pull-up “ON”	-5.0	-20	-40	μA
I _{IL}	“L” input current RESET	V _I = V _{SS}			-5.0	μA
I _{IL}	“L” input current XIN	V _I = V _{SS}		-4.0		μA

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Table 16 Electrical characteristics (Mask ROM version)

(Vcc = 1.8 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
VRAM	RAM hold voltage	When clock is stopped	1.8		5.5	V	
ICC	Power source current	Through mode, Vcc = 5 V f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors "OFF", A-D converter in operating		5.1	7.5	mA	
		Through mode, Vcc = 5 V f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors "OFF", A-D converter stopped		1.0	2.0	mA	
		Low-speed mode, Vcc = 5 V, Ta ≤ 55 °C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "OFF"		14	21	μA	
		Low-speed mode, Vcc = 5 V, Ta = 25 °C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "OFF"		6	10	μA	
		Low-speed mode, Vcc = 3 V, Ta ≤ 55 °C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "OFF"		7	12	μA	
		Low-speed mode, Vcc = 3 V, Ta = 25 °C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "OFF"		3	6	μA	
		All oscillation stopped (in STP state) Output transistors "OFF"	Ta = 25 °C		0.1	1.0	μA
			Ta = 85 °C			10	μA

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

A-D Converter Characteristics

Table 17 A-D converter characteristics (Mask ROM version)

(Vcc = 2.2 to 5.5 V, Vss = AVss = 0 V, Ta = -20 to 85°C, Port state = stopped, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Differential non-linearity error	VCC = VREF = 5 V			±1	LSB
	Non-linearity error				±1	
	Off-set error				±3	
	Full-scale error				±5	
	Differential non-linearity error	• VCC = VREF = 2.2 V, AD clock frequency = 250 kHz • VCC = VREF = 2.3 V, AD clock frequency = 500 kHz • VCC = VREF = 2.4 V, AD clock frequency = 1 MHz • VCC = VREF = 2.5 V, AD clock frequency = 2 MHz • VCC = VREF = 2.5 V, AD clock frequency = 4 MHz • VCC = VREF = 2.6 V, AD clock frequency = 8 MHz			±1	LSB
	Non-linearity error				±1	
	Off-set error				±2	
	Full-scale error				±3	
Tconv	Conversion time	AD conversion clock selection bit :Frequency not divided, 10bitAD mode			tc(XIN)X121 (Note)	µs
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference input current	VREF = 5 V	50	150	200	µA
I _A	Analog input current				5.0	µA

Note: When "Frequency/2, 4 or 8" is selected by the AD conversion clock selection bit, the above conversion time is multiplied by 2, 4 or 8.

LCD Power Supply Characteristics

Table 18 LCD power supply characteristics (when connecting division resistors for LCD power supply)

(Vcc = 1.8 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min.	Typ.	Max.			
RLCD	Division resistor for LCD power supply (Note)	RSEL = "10"		200		kΩ		
		RSEL = "11"		5				
		LCD drive timing A	LCD circuit division ratio = divided by 1	RSEL = "01"			120	
				RSEL = "00"			90	
			LCD circuit division ratio = divided by 2	RSEL = "01"			150	
				RSEL = "00"			120	
			LCD circuit division ratio = divided by 4	RSEL = "01"			170	
				RSEL = "00"			150	
		LCD drive timing B	LCD circuit division ratio = divided by 1	RSEL = "01"			150	
				RSEL = "00"			120	
			LCD circuit division ratio = divided by 2	RSEL = "01"			170	
				RSEL = "00"			150	
			LCD circuit division ratio = divided by 4	RSEL = "01"			190	
				RSEL = "00"			170	
LCD circuit division ratio = divided by 8	RSEL = "01"		190					
	RSEL = "00"		190					

Note: The value is the average of each one division resistor.

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Timing Requirements And Switching Characteristics

Table 19 Timing requirements 1

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	Main clock input cycle time (XIN input)	125			ns
twH(XIN)	Main clock input "H" pulse width	45			ns
twL(XIN)	Main clock input "L" pulse width	40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	250			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	105			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	105			ns
twH(INT)	INT0-INT2 input "H" pulse width	80			ns
twL(INT)	INT0-INT2 input "L" pulse width	80			ns
tc(SCLK)	Serial I/O1, 2 clock input cycle time (Note)	800			ns
twH(SCLK)	Serial I/O1, 2 clock input "H" pulse width (Note)	370			ns
twL(SCLK)	Serial I/O1, 2 clock input "L" pulse width (Note)	370			ns
tsu(RxD-SCLK)	Serial I/O1, 2 input setup time	220			ns
th(SCLK-RxD)	Serial I/O1, 2 input hold time	100			ns

Note : When bit 6 of address 0FE016 or 0FE316 is "1" (clock synchronous).
 Divide this value by four when bit 6 of address 0FE016 or 0FE316 is "0" (UART).

Table 20 Timing requirements 2

(Vcc = 1.8 to 4.0 V, Vss = 0 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	Main clock input cycle time (XIN input)	125			ns
twH(XIN)	Main clock input "H" pulse width	45			ns
twL(XIN)	Main clock input "L" pulse width	40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	11000/(15×Vcc-16)			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	tc(CNTR)/2-20			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	tc(CNTR)/2-20			ns
twH(INT)	INT0-INT2 input "H" pulse width	230			ns
twL(INT)	INT0-INT2 input "L" pulse width	230			ns
tc(SCLK)	Serial I/O1, 2 clock input cycle time (Note)	2000			ns
twH(SCLK)	Serial I/O1, 2 clock input "H" pulse width (Note)	950			ns
twL(SCLK)	Serial I/O1, 2 clock input "L" pulse width (Note)	950			ns
tsu(RxD-SCLK)	Serial I/O1, 2 input setup time	400			ns
th(SCLK-RxD)	Serial I/O1, 2 input hold time	200			ns

Note : When bit 6 of address 0FE016 or 0FE316 is "1" (clock synchronous).
 Divide this value by four when bit 6 of address 0FE016 or 0FE316 is "0" (UART).

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Table 21 Switching characteristics 1

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{wH} (SCLK)	Serial I/O1, 2 clock output "H" pulse width	t _c (SCLK)/2-30			ns
t _{wL} (SCLK)	Serial I/O1, 2 clock output "L" pulse width	t _c (SCLK)/2-30			ns
t _d (SCLK-TxD)	Serial I/O1, 2 output delay time (Note 1)			140	ns
t _v (SCLK-TxD)	Serial I/O1, 2 output valid time (Note 1)	-30			ns
t _r (SCLK)	Serial I/O1, 2 clock output rising time			30	ns
t _f (SCLK)	Serial I/O1, 2 clock output falling time			30	ns
t _r (CMOS)	CMOS output rising time (Note 2)		10	30	ns
t _f (CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1: When the P-channel output disable bit (bit 4 of address 0FE116 or 0FE416) is "0."

2: The XOUT, XCOUT pins are excluded.

Table 22 Switching characteristics 2

(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{wH} (SCLK)	Serial I/O1, 2 clock output "H" pulse width	t _c (SCLK)/2-50			ns
t _{wL} (SCLK)	Serial I/O1, 2 clock output "L" pulse width	t _c (SCLK)/2-50			ns
t _d (SCLK-TxD)	Serial I/O1, 2 output delay time (Note 1)			350	ns
t _v (SCLK-TxD)	Serial I/O1, 2 output valid time (Note 1)	-30			ns
t _r (SCLK)	Serial I/O1, 2 clock output rising time			50	ns
t _f (SCLK)	Serial I/O1, 2 clock output falling time			50	ns
t _r (CMOS)	CMOS output rising time (Note 2)		20	50	ns
t _f (CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1: When the P-channel output disable bit (bit 4 of address 0FE116 or 0FE416) is "0."

2: The XOUT, XCOUT pins are excluded.

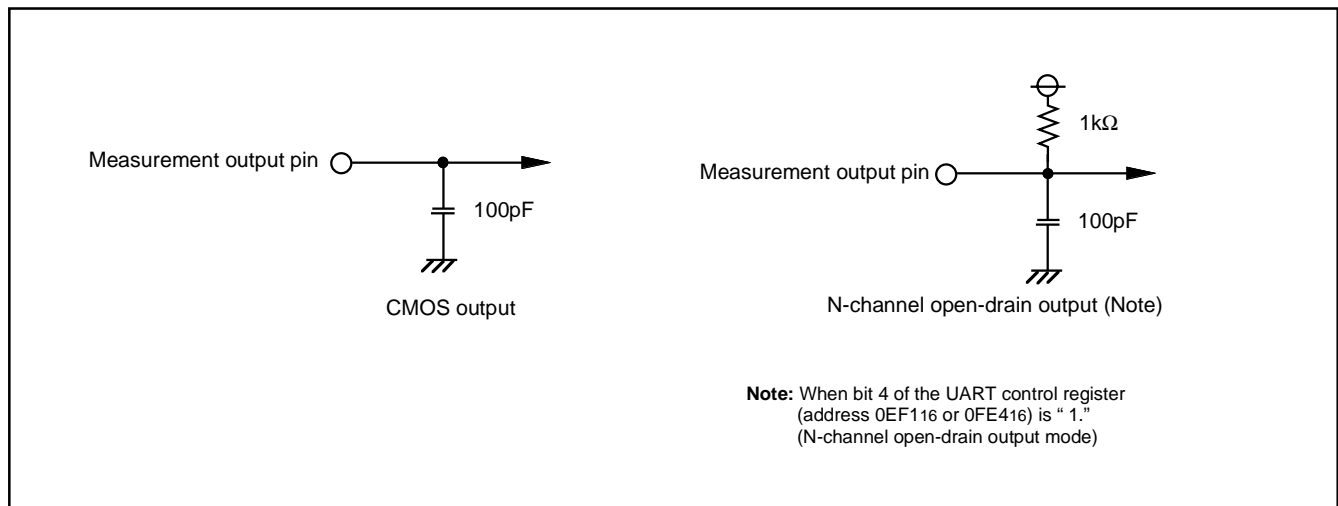


Fig. 56 Circuit for measuring output switching characteristics

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

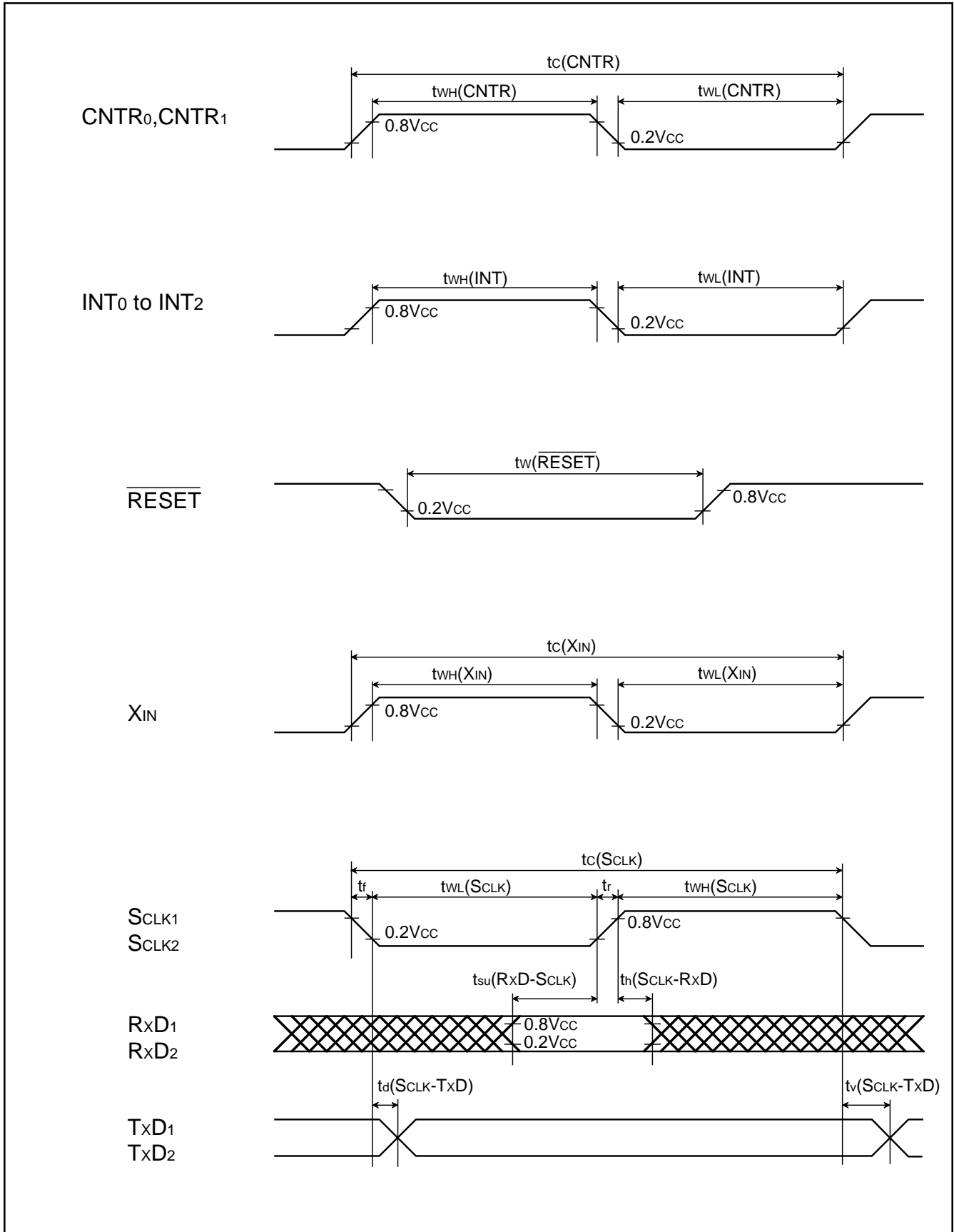


Fig. 57 Timing chart

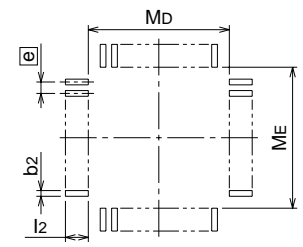
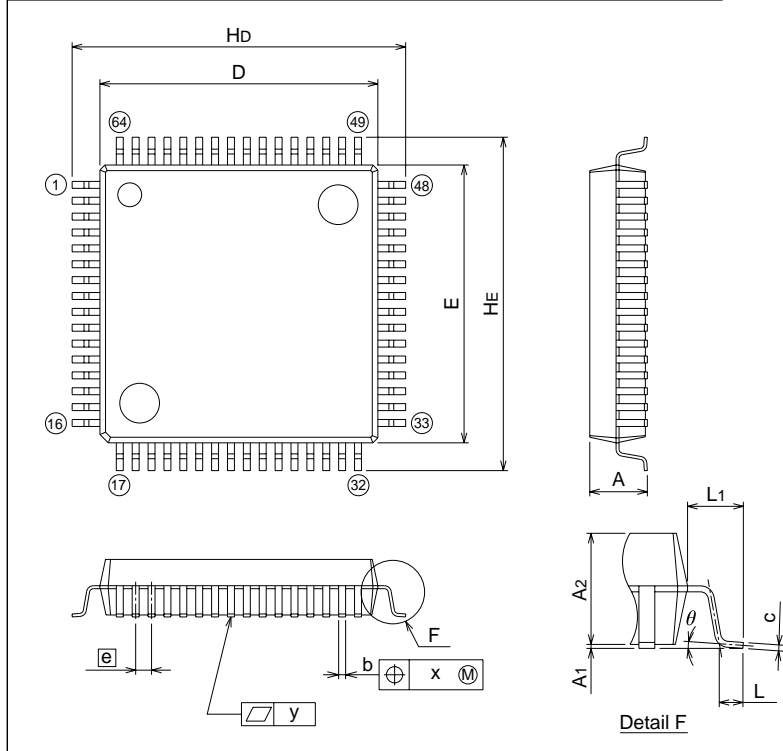
PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

PACKAGE OUTLINE

64P6N-A

Plastic 64pin 14X14mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP64-P-1414-0.80	-	1.11	Alloy 42



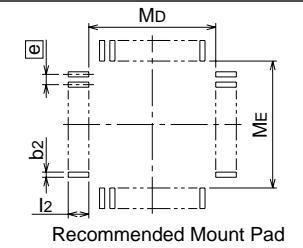
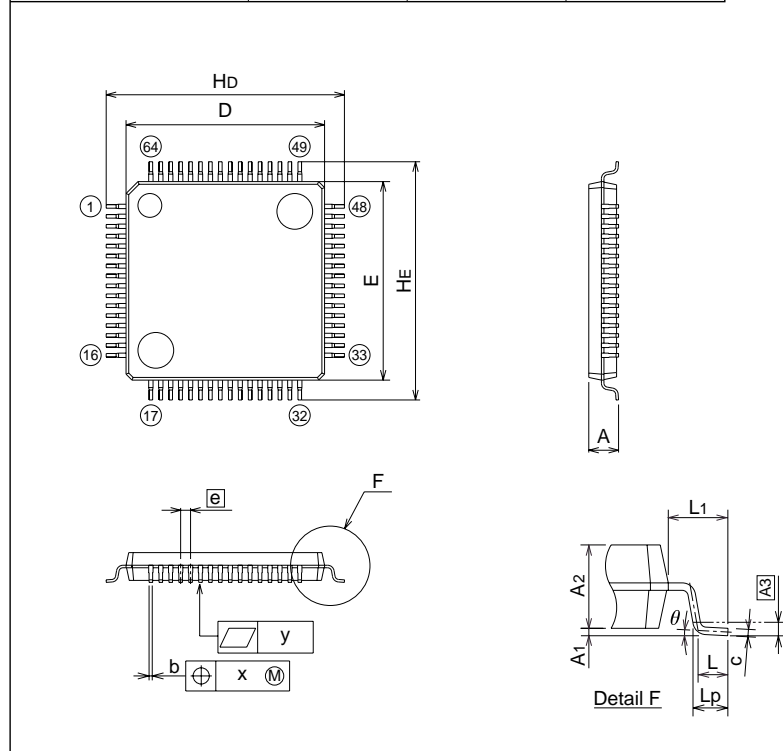
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	-	0.8	-
Hd	16.5	16.8	17.1
HE	16.5	16.8	17.1
L	0.4	0.6	0.8
L1	-	1.4	-
x	-	-	0.2
y	-	-	0.1
θ	0°	-	10°
b2	-	0.5	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	14.6	-

64P6Q-A

Plastic 64pin 10X10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.50	-	-	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	-	0.5	-
Hd	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
θ	0°	-	10°
b2	-	0.225	-
l2	1.0	-	-
MD	-	10.4	-
ME	-	10.4	-

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.



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- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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REVISION DESCRIPTION LIST

38C2 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	000830
1.1	P53 Table 12 Recommended operating condition Parameter of VIH, VIL : "XIN" (wrong) → "XIN, XCIN" (correct)	000901